Abstract—A novel design technique employing CMOS Current Feedback Operational Amplifier (CFOA) is presented. The feature of consumption very low power in designing pseudo-OTA is used to decreasing the total power consumption of the proposed CFOA. This design approach applies pseudo-OTA as input stage cascaded with buffer stage. Moreover, the DC input offset voltage and harmonic distortion (HD) of the proposed CFOA are very low values compared with the conventional CMOS CFOA due to the symmetrical input stage. P-Spice simulation results are obtained using 0.18µm MIETEC CMOS process parameters and supply voltage of ±1.2V, 50µA biasing current. The p-spice simulation shows excellent improvement of the proposed CFOA over existing CMOS CFOA. Some of these performance parameters, for example, are DC gain of 62. dB, open-loop gain bandwidth product of 108 MHz, slew rate (SR+) of +71.2V/µS, THD of -63dB and DC consumption power (PC) of 2mW.

Keywords—Pseudo-OTA used CMOS CFOA, low power CFOA, high-performance CFOA, novel CFOA.

I. INTRODUCTION

In recent years, great interest has been devoted to the analysis and design of current feedback op-amp and current-conveyor integrated circuits, mainly because these circuits exhibits better performance, have particularly higher speed and better bandwidth than classic voltage-mode operational amplifiers (VOA) [1]. However, the conventional CMOS CFOA design is still facing certain problems, first, the offset voltage on the current feedback cannot be made zero. CFOA usually adopts an analog buffer as the input stage. As a result, the non-inverting input has very high impedance while the inverting input has very low impedance. Hence, the CFOA's offset is higher than folded cascade voltage amplifier (VFA) Design. Second, the constant bandwidth feature of the CFOA is still facing certain problems, first, the offset voltage on the current feedback cannot be made zero. CFOA usually adopts an analog buffer as the input stage. As a result, the non-inverting input has very high impedance while the inverting input has very low impedance. Hence, the CFOA's offset is higher than folded cascade voltage amplifier (VFA) Design. Second, the constant bandwidth feature of the CFOA is still facing certain problems, first, the offset voltage on the current feedback cannot be made zero. CFOA usually adopts an analog buffer as the input stage. As a result, the non-inverting input has very high impedance while the inverting input has very low impedance. Hence, the CFOA's offset is higher than folded cascade voltage amplifier (VFA) Design. Second, the constant bandwidth feature of the CFOA is still facing certain problems. However, for the pseudo-OTA shown in Fig. 1, Common Mode (CM) voltage gain is equal to the differential mode (DM) voltage gain (= gm R0), i.e., CMRR= DM=CM=1. This large CM, in pseudo-differential structures, can lead to huge common-mode variations at the OTA outputs unless a fast and strong CMFB is used [14].

II. THEORETICAL BACKGROUND OF PSEUDO-OTA

Fully-differential OTA is typical pair with the tail current source, and pseudo-differential is based on two independent inverters without a tail current source as shown in Fig. 1 avoiding the voltage drop across the tail current source in a PD structure allows achieving wider input range and makes the architecture attractive for low voltage applications. Removing the tail current source, however, results in larger common-mode gain (ACM). In an FD structure, the common-mode gain can be reduced by increasing the output resistance of the bias current source. However, for the pseudo-OTA shown in Fig. 1, Common Mode (CM) voltage gain is equal to the differential mode (DM) voltage gain (= gm R0), i.e., CMRR= DM=CM=1. This large CM, in pseudo-differential structures, can lead to huge common-mode variations at the OTA outputs unless a fast and strong CMFB is used [14].
Using a balanced configuration with two single-ended transconductances reduces ACM at low frequency to the order of unity. This approach adds more load to the driving stage due to the connection two input transistors, thus doubling the input capacitance. The same also applies to the case of the common-mode feed forward (CMFF) technique. A common-mode gain, at low frequency, is given by \[ A_{cm} = \frac{v_{acm}}{v_{icm}} = \frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \approx g_{m1}/g_{m2} \] \[ (1) \]

The operation of pseudo-OTA consists of one differential pair consisting of NMOS transistors M1 and M2; MOS transistors M3 and M4 provide the DC bias. The pseudo-OTA characterized by performance such as high DC voltage gain, wide gain bandwidth product, low noise and consumption power [15]. The gain of the pseudo-OTA is given by: \[ V_{o}/V_{in} = G_{m1}R_{D} \]

and the gain bandwidth product is given by: \[ GBW = G_{m1}/C_{L} \] \[ (2) \]

\[ (3) \]

where \( G_{m1} \) is the transconductance of transistor M1 and \( R_{D} \) (output resistance) \((= (R_{D} \text{ looking into the drain of } M1)/ (R \text{ looking into transistor into the drain of } M4))\). After applying the design strategy clarified previously, the design parameters in strong inversion region, the gate-dimensions, and biasing currents, of MOS transistors are summarized in Table I.

<table>
<thead>
<tr>
<th>Transistors no.</th>
<th>Gate dimensions and biasing currents</th>
<th>Biasing Current(μA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>W(μm) 12.0  L(μm) 0.18</td>
<td>25</td>
</tr>
<tr>
<td>M2</td>
<td>W(μm) 16.1  L(μm) 0.18</td>
<td>25</td>
</tr>
<tr>
<td>M3</td>
<td>W(μm) 11.59 L(μm) 0.18</td>
<td>50</td>
</tr>
<tr>
<td>M4</td>
<td>W(μm) 6.21  L(μm) 0.18</td>
<td>50</td>
</tr>
<tr>
<td>M5</td>
<td>W(μm) 9.5   L(μm) 0.35</td>
<td>50</td>
</tr>
<tr>
<td>M6</td>
<td>W(μm) 2.0   L(μm) 0.18</td>
<td>50</td>
</tr>
<tr>
<td>M7</td>
<td>W(μm) 23.8  L(μm) 0.18</td>
<td>50</td>
</tr>
<tr>
<td>M8</td>
<td>W(μm) 6.0   L(μm) 0.18</td>
<td>50</td>
</tr>
</tbody>
</table>

In our proposed CFOA using feedback technique of pseudo-OTA by connecting the positive output terminal to the negative input terminal as shown in block diagram of Fig. 2. This technique called current feedback OTA technique [16]. This approach represents input stage of proposed CFOA and cascading with buffer stage as shown in the schematic circuit of Fig. 3.

### III. SIMULATION RESULTS

A new alternative CMOS CFOA with the high-performance operation, very low input offset voltage, and low distortion are proposed in this paper. Since, the high-frequency parameters such as voltage gain, (-3dB) bandwidth, slew rate (SR), settling time (ts) and gain bandwidth product (GBW) are improved. Fig. 3 clarifies the improvement in the open loop voltage gain and gain bandwidth product (GBW) of the proposed CMOS CFOA. Also, the magnitude curve in Fig. 4 shows the frequency response (variation of frequency against the voltage gain and phase curve shows the variation of frequency against the phase shift between input and output voltage.

![Fig. 3 Schematic circuit of proposed CFOA based on pseudo-OTA](image)

The value of output impedance of buffer stage is decreased drastically due to using cross-coupled buffer stage. Fig. 5 indicate that the improvement in closed loop (-dB bandwidth) of the proposed CMOS CFOA, since the values of (-dB bandwidth) is 108 MHz compared with 46.2 MHz with introduce the closed loop resistors \( R_F=1KΩ \) and \( R_I=1KΩ \). The value of voltage gain will increase with decreasing in the (-3db) bandwidth due to change the value of \( R_F \) and keep the value of \( R_I \) is constant. The slow rate of CMOS and CFOA are measured from Fig. 6. DC characteristics of CMOS CFOA is shown in Fig. 7, we note that there is a large enhancement in linearity of DC characteristics of the CMOS CFOA due to the symmetry in the operation of the fully differential input stage of the pseudo-CFA OTA. Moreover, we note that the value of input offset voltage is -0.1 mV due to the symmetry in the input stage (inverting and non-inverting inputs) of the proposed CMOS CFOA.
(GBW), (-3dB) bandwidth, phase margin (PM), and total harmonic distortion (HD). Simulation results of proposed CMOS CFOA confirmed the theoretical concepts in previous sections.

### TABLE II

**PERFORMANCE PARAMETERS OF THE PROPOSED CMOS CFOA AS INPUT RESISTOR (R_I) IS VARIED**

<table>
<thead>
<tr>
<th>R_I (KΩ)</th>
<th>-3dB B.W (MHz)</th>
<th>GBW (MHz)</th>
<th>PM (deg.)</th>
<th>THD (dB)</th>
<th>Av (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>79.6</td>
<td>108</td>
<td>49.9°</td>
<td>-67.0</td>
<td>5.9</td>
</tr>
<tr>
<td>0.3</td>
<td>32.7</td>
<td>89.2</td>
<td>48.6°</td>
<td>-65.0</td>
<td>12.5</td>
</tr>
<tr>
<td>0.1</td>
<td>10.7</td>
<td>81.8</td>
<td>46.0°</td>
<td>-41.7</td>
<td>20.4</td>
</tr>
<tr>
<td>0.01</td>
<td>1.0</td>
<td>78.6</td>
<td>45.0°</td>
<td>-41.0</td>
<td>39.1</td>
</tr>
</tbody>
</table>

**Fig. 4** Open-loop frequency response of the proposed CMOS CFOA

**Fig. 5** Closed-loop frequency response of the proposed CMOS CFOA as R_I is varied from 0.01KΩ to 1 KΩ

**Fig. 6** Transient response of the proposed CMOS CFOA

### IV. CONCLUSION

A new design technique of the CMOS CFOA with attractive features for high frequency, low offset voltage, and low distortion is proposed in this paper. The proposed design based on cross-coupled buffer stage that connected as the output stage of the CMOS CFOA. Since this technique operates on logic transition concept that gives the high speed, symmetry operation of the output signal and high current drive capability of proposed CMO CFOA. The high speed operation improved high performance parameters such as gain bandwidth (GBW), (-3dB) bandwidth, slew rate (SR) and settling time (t_s) with ensure the phase margin (PM) in acceptable value that keep the stability of operation. Moreover, the symmetry of input differential of pseudo-CFA OTA technique decreased the distortion in the output signal and improved (DC) characteristics of CMOS CFOA. Also to that using pseudo-OTA as the input stage of CMOS CFOA make the symmetry of inverting and non-inverting inputs that reduce input offset voltage. The trans-impedance node (Z) of the CMOS CFOA gained high value due to cascading transistors of CFA OTA. This feature is very important for design CMOS CFOA with high gain. We can summarize our conclusion by saying that the proposed CMOS CFOA with
symmetry of the input stage and symmetry of the output stage will gain CMOS CFOA attractive features for many high frequencies, low distortion, low input offset voltage applications. Also, the CMFB circuit is avoided due to the connection of the output terminal of the pseudo-OTA to input terminal to propose current feedback OTA.

REFERENCES


