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SCR-Stacking Structure with High Holding Voltage for I/O and Power Clamp

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Abstract**—**In this paper, we proposed a novel SCR (Silicon Controlled Rectifier) - based ESD (Electrostatic Discharge) protection device for I/O and power clamp. The proposed device has a higher holding voltage characteristic than conventional SCR. These characteristics enable to have latch-up immunity under normal operating conditions as well as superior full chip ESD protection. The proposed device was analyzed to figure out electrical characteristics and tolerance robustness in term of individual design parameters (D1, D2, D3). They are investigated by using the Synopsys TCAD simulator. As a result of simulation, holding voltage increased with different design parameters. The holding voltage of the proposed device changes from 3.3V to 7.9V. Also, N-Stack structure ESD device with the high holding voltage is proposed. In the simulation results, 2-stack has holding voltage of 6.8V and 3-stack has holding voltage of 10.5V. The simulation results show that holding voltage of stacking structure can be larger than the operation voltage of high-voltage application.

Keywords**—**ESD, SCR, holding voltage, stack, power clamp.

I. Introduction

THE development of semiconductor process technologies brought about the miniaturization of ICs(Integrated devices), but the failure of device by ESD(Electrostatic Discharge) is becoming a more serious problem. Furthermore, with the increasing demand for analog and high-voltage IC technologies, the ESD protection device is being regarded as important for the reliability of IC [1]. The silicide-blocked ggNMOS (Gate Grounded NMOS) is the common ESD protection structure [2]. But due to the low current driving capability, ggNMOS consumes a relatively large silicon area. Hence, significant parasitic effects are present, which make ggNMOS devices the non-optimum solution for high ESD robustness, high frequency, large pin count, and area-sensitive IC chips. In the meantime, SCR (Silicon Controlled Rectifier)-based ESD protection device can effectively discharge the ESD surge because it has high current driving capacity compared to area due to the positive feedback structure of the parasitic NPN/PNP bipolar transistor inside the silicon substrate. However, the parasitic NPN/PNP bipolar transistor is vulnerable to latch-up in high-voltage applications because it has a low holding voltage of about 2 V which is a turn-on voltage [3]. It is hard to effectively discharge ESD current before malfunction of core device and destruction of gate oxide. Some SCR-based devices (LVTSCR, GGSCR, etc.) have been proposed in order to have a low triggering voltage [4], [5]. However, due to low holding voltage, they have still transient-induced latch-up problem [6]. The latch-up issue can be overcome by increasing the holding current or holding voltage. Consequently, SCR is difficult to design ESD protection in high voltage application [7]-[10]. In this paper, we will introduce the SCR based ESD protection device with a high holding voltage. Moreover, a SCR stacking structure comprised of SCR with a high holding voltage is proposed.

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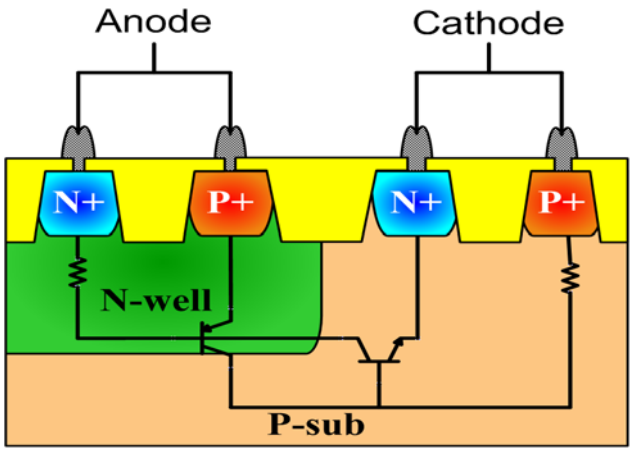
II. Single SCR-Based ESD Protection Device with High Holding Voltage

A. Device Description

Cross section of conventional SCR is shown in Fig. 1 (a). When ESD surge is applied to SCR, junction between N-well and P-well is reverse biased. As anode voltage increases, the junction goes into avalanche breakdown. Generated current makes voltage drop and NPN parasitic bipolar transistor turns on. After NPN transistor turns on, its current makes PNP transistor turns on. These NPN/PNP transistors operate in positive feedback and it makes relatively low holding voltage about 2V as shown in Fig. 1 (c). This low holding voltage leads to latch-up problem during normal operation condition. Also, high trigger voltage leads to gate oxide breakdown of internal devices. Therefore, we propose modified SCR-based ESD devices with high holding voltage [11].



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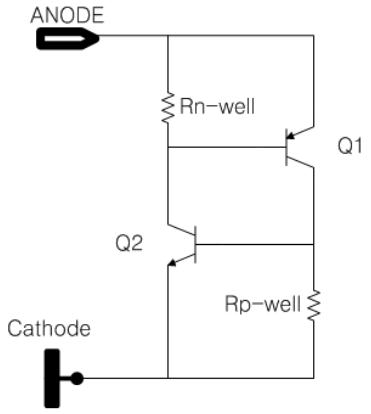

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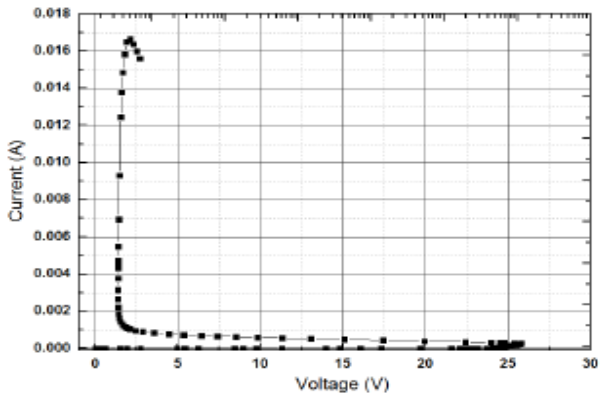
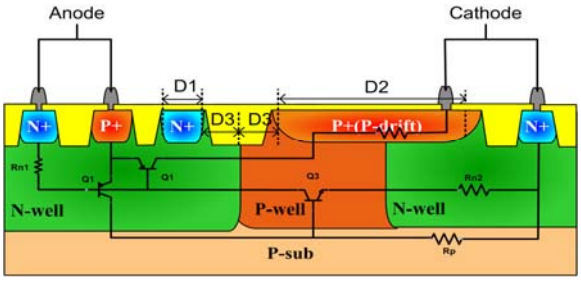


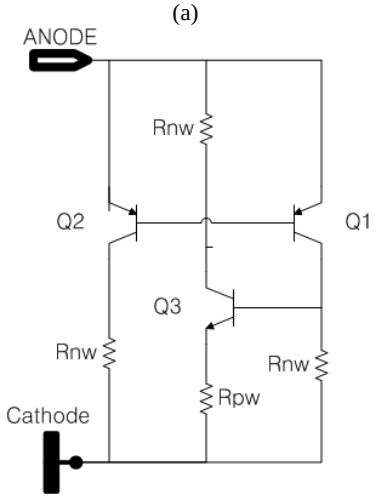
(c)

Fig. 1 Cross section of conventional SCR ESD protection devices (a) cross-sectional view and equivalent devices (b), I-V characteristic curve of conventional SCR ESD protection devices (c)

Proposed SCR-based ESD protection device was transformed and the floating n+ expansion area inserted in n-well area was added. Then, p+ cathode (p-drift) was expanded into the p-well area and the base width of the NPN/PNP bi-pole parasitically generated in SCR was expanded to reduce the current gain (Beta) and thus raise holding voltage. In addition, a resistant role on a discharge path was designed by covering the cathode phase with n-well and inserting a well-resistor, and the emitter injection efficiency of the parasitic NPN bipolar was reduced to raise the holding voltage. The operation principle of the proposed device is as follows: When ESD phenomenon occurs from the anode electrode, the junction of the n-well and the p-well is reverse biased. At this moment, avalanche break down occurs due to high electric field between the junctions. And EHP (Electron-Hole Pair) is generated by avalanche breakdown, when hole current flows to p-drift junction through parasitic PNP bipolar Q2, and the p-well electric potential increases. The emitter-base junction of parasitic NPN bipolar Q3 becomes forward-biased due to the raised electric potential of the p-well, and NPN bipolar Q3 turns on. When Q3 turns on, Q3 current causes a voltage drop in Rn1, and PNP bipolar Q1 also turns on. Q1 current also results in a voltage drop at Rp, which helps Q3 turn on. In this process there is no need to supply bias to Q3 any longer due to Q3 current. The holding voltage of the ESD protection device relies on the space charge neutralization in the base area between NPN and PNP due to the carrier inflowing from the NPN/PNP bipolar emitter area. Thus, the bipolar base width and the p-drift area width are very important. To Analyze holding voltage properties associated with this, design parameters D1, D2 and D3 have been set. Individual design parameters include floating n+ area (D1) associated with PNP/NPN bipolar base width, p-drift junction length (D2), n-well distance in floating n+ area, and p-well length (D3) in p-drift area.



(a)

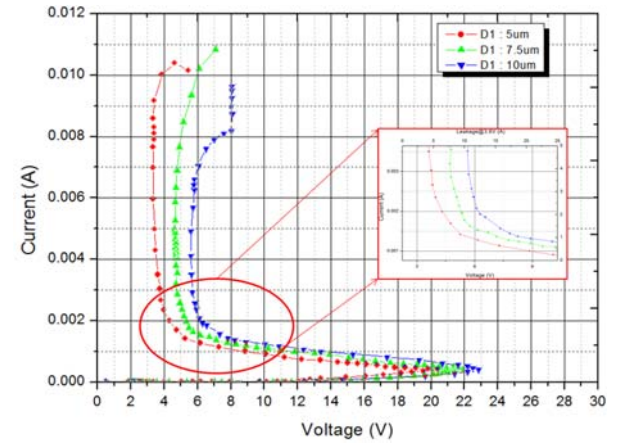


(b)

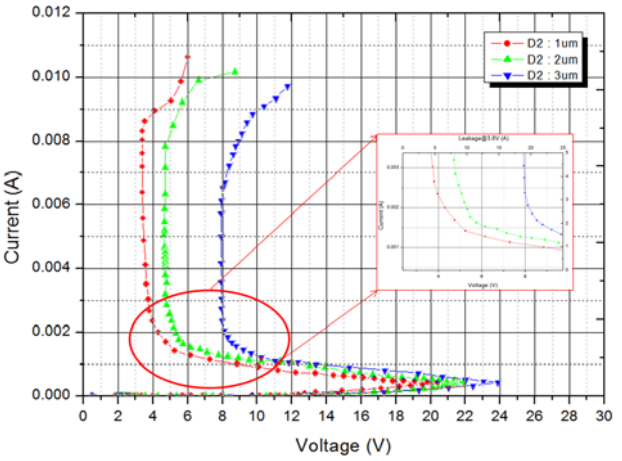
Fig. 2 Cross section of the proposed SCR-based ESD protection device (a) cross-sectional view and equivalent device (b)

B. Analysis of a Single SCR-Based ESD Protection Device

Before a stacked SCR-based device with high holding voltage can be composed, we tried to analyze the holding voltage trend of the single SCR-based ESD protection device with different design parameters, D1, D2 and D3 (shown in Fig. 2). They are investigated by using the Synopsys TCAD simulator



(a)



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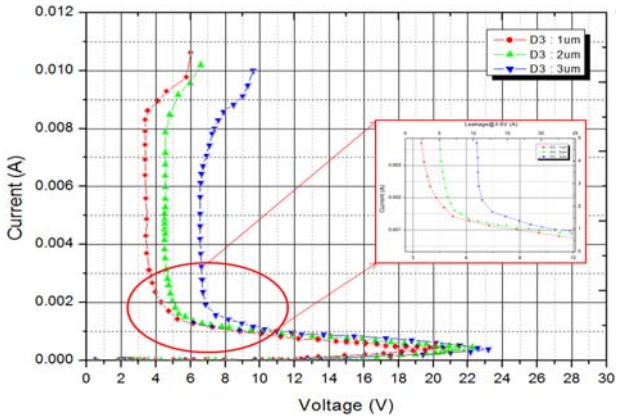

(c)

Fig. 3 The Simulated I-V characteristics of a single SCR-based device with different design parameters of (a) D1 variation, (b) D2 variation and (c) D3 variation

All the design parameters of a SCR-based device in the simulation are fixed at a similar value except the design parameters D1, D2 and D3. The simulated I-V characteristics of a single SCR-based device with different design parameters are shown in Fig. 2 (a). Fig. 3 (a) indicates length changes in the graph design parameter D1: 5um, 7.5um and 10um. The more the design parameter D1 increases, holding voltages increased up to 3.3V, 4.7V and 5.6V, respectively, as current gains decreases with the increases in the base width of the PNP bipolar. Fig. 3 (b) shows a graph when the design parameter D2 changes in length: 1um, 2um and 3um. As the design parameter D2 gradually increases, the holding voltage increases from 3.3V to 7.9V with the decrease in current gain. On the contrary, the second breakdown current decreases because high resistance of discharge path leads to high power dissipation, so current driving capability decreases. Fig. 3 (c) is graph showing length changes in design parameter D3: 1um, 3um and 5um. As the design parameter D3 gradually increases, the holding voltage increase from 3.3V to 6.5V with the increase in NPN/PNP bipolar base width. Simulation results for trigger voltage and holding voltage are shown in Table I.

TABLE I
SIMULATION RESULTS OF THE PROPOSED DEVICE

D1	**Trigger Voltage (Vt)**	**Holding Voltage (Vh)**
5 um	20.5 V	3.3 V
7.5 um	21.8 V	4.7 V
10 um	22.9 V	5.6 V
D2	**Trigger Voltage (Vt)**	**Holding Voltage (Vh)**
1 um	20.5 V	3.3 V
2 um	21.8 V	4.8 V
3 um	23.8 V	7.9 V
D3	**Trigger Voltage (Vt)**	**Holding Voltage (Vh)**
1 um	20.5 V	3.3 V
3 um	22.1 V	4.5 V
5 um	23.1 V	6.5 V

III. STACKED SCR-BASED ESD PROTECTION DEVICE

Stacked SCR-based devices can be accomplished by connecting two or more of the aforementioned SCR-based devices. The cross sectional view of the stacking of three SCR-based devices is shown in Fig. 4. It is verified by Synopsys TCAD simulation tool and result of proposed protection devices are shown in Fig. 5. When stack number increases, the Trigger voltage of 1-stack is 20.5V, 2-stack is 41V and 3-stack is 58V. The holding voltage of 1-stack is 3.3V, 2-stack is 6.8V and 3-stack is 10.5V. Table II is shown simulation results.

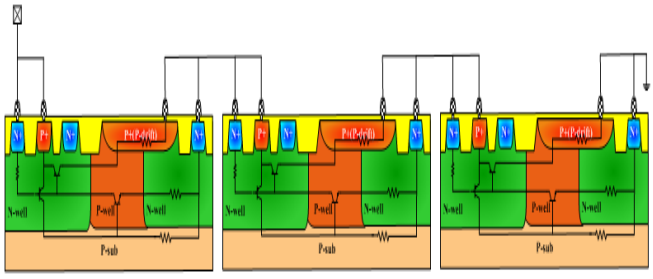

Fig. 4 Cross-sectional view of 3-stacking SCR-based Device

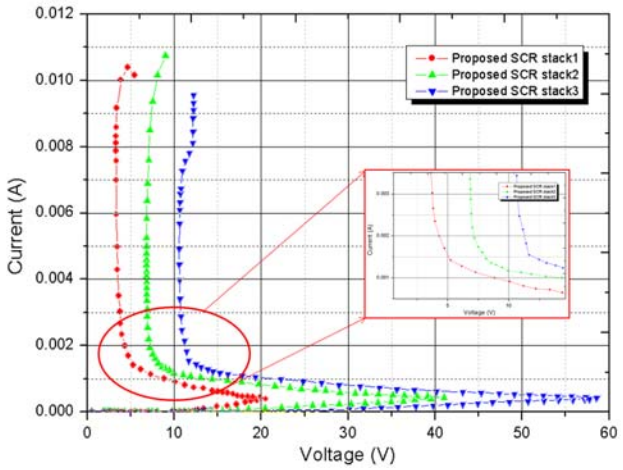

Fig. 5 The Simulated I-V curve characteristics of the proposed n-Stack structure

TABLE II
SIMULATION RESULTS OF STACKED PROPOSED DEVICE

N-stack	Trigger Voltage(Vt)	Holding Voltage(Vh)
1-stack	20.5 V	3.3 V
2-stack	41 V	6.8 V
3-stack	58 V	10.5 V

IV. CONCLUSION

This paper presented SCR-based ESD protection devices with high holding voltage for I/O and power clamp. In comparison to conventional SCR, these proposed devices have high holding voltage. Also, these used SCR stacking structure with a high holding voltage for a latch-up immune high voltage application. In TCAD simulation results, the holding voltage of the single proposed SCR-based device changes from 3.3 V to 7.9V. By using the proposed SCR-based device n-Stack structure, the ESD protection device has the advantage of holding voltage. From the simulation, holding voltage of each stack can be identified as 3.3V, 6.8V and 10.5V respectively. When using n-stack structure, it is improved that approximately n-fold holding voltage as the simulation results. Thus, the proposed ESD protective device has latch-up immunity characteristics due to the high holding voltage, and the high robustness is expected to improve reliability of intergared devices more.

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