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Power Factor Correction Based on High Switching Frequency Resonant Power Converter

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***Abstract*—**This paper presents Buck-Boost converter topology to maintain the input power factor by using the power factor stage control and regulation stage control. Suppose, if we are using the RL load the power factor will be reduced due to the presence of total harmonic distortion in the current wave. To improve the power factor the current waveform should follow the fundamental component of the voltage waveform. These can be achieved by using the high - frequency power converter. Based on the resonant circuit the converter is able to perform the function of Buck, Boost, and buck-boost converter. Here ,we have used Buck-Boost converter, because, the buck-boost converter has more advantages than the boost converter. Here the switching action of the power converter can take place by using the external zero comparator PFC stage control. The power converter consisting of the resonant circuit which is used to control the output voltage gain of the converter. The power converter is operated at a very high switching frequency in the range of 400KHz in order to overcome the switching losses of the power converter. Due to presence of high switching frequency, the power factor will improve. Therefore, the total harmonics distortion present in the current waveform has also reduced. These results has generated in the form of simulation by using MATLAB/SIMULINK software. Similar to the Buck and Boost converters, the operation of the Buck-Boost has best understood, in terms of the inductor's "reluctance" for allowing rapid change in current, which also reduces the Total Harmonic Distortion (THD) in the input current waveform, which can improve the input Power factor, based on the type of load used.

***Keywords*—**Buck-boost converter, High switching frequency, Power factor correction, power factor correction stage Regulation stage, Total harmonic distortion (THD).

I. Introduction

CUSTOMARILY, the simplest approach is to use a diode rectifier circuit with an output storage capacitor as shown in Fig.1.However, this capacitor is charged near to the peak value of AC input voltage which is shown in the Fig.2.

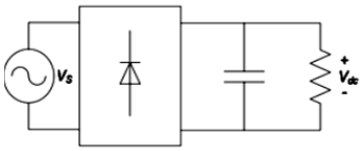

Fig. 1 Diode rectifier with a capacitor connected at the DC output

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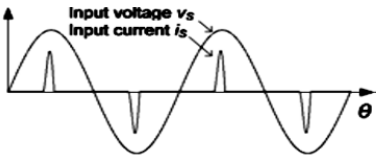

Fig. 2 Input voltage and current waveforms

As a result, the input pulsating current of large magnitude occurs near the peak of the AC input voltage. Due to the presence of discontinuous current in the wireless system, the power will not flow from the primary side of the WPT system to the secondary side of the system [1], [4], [5], [10]. Such diode rectifiers draws highly distorted current from the AC power source and results in a poor input power factor(PF) [3], [6]. The energy efficiency and power transfer capability of a poor PF system is comparatively low, because of high conduction loss in the power converters and transmission wires [7]-[9]. Additionally, the distorted current has a rich higher order harmonic contents which cause the emission of electromagnetic interference (EMI) that affects the operation of other electronic equipment connected together [2]. In a proposed system, the power electronic converter, such as a buck- boost converter has used to shape the input AC current drawn by the rectifier to be sinusoidal and in phase with the AC voltage.

II. Block Diagram of Existing System

The input AC supply has given to the diode rectifier circuit which converts dc supply. The input AC voltage has also given to the PFC stage control to generate the control signals of switches in the PFC stage through the driver circuit.

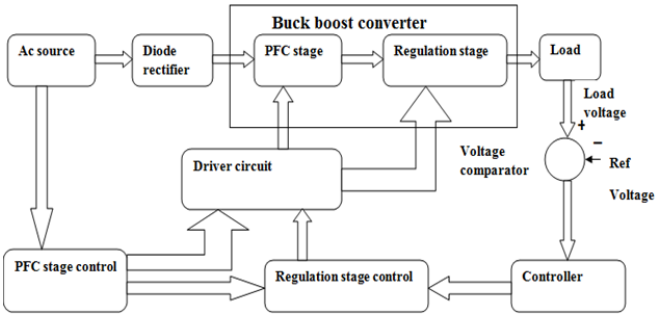

Fig. 3 Block Diagram of Existing System

The output of the PFC stage control is also given to the Regulation stage control. The output of Diode rectifier circuit is given to the PFC stage and Regulation stage which contains power converter i.e. Boost converter. The Regulated output is

given to the load. The load voltage is sensed and fed to the voltage comparator which compares the actual load voltage with reference voltage and generates the Error signal. The Error voltage is applied to a compensator to generate the threshold voltage Vcr,min for the resonant capacitors C_{r1} and C_{r2}. The low resonant capacitor voltage is applied to the regulation stage control after that voltages V_{cr1} and V_{cr2} are being sensed and compared with V_{cr}min to generate the PWM signal for the regulation stage. Here the load is resistive load. So based on the load condition, the power factor will be improved. By considering an example as a 400-kHz AC transmission system, the current shaping technology gives that the power switch has to operate in ten MHz. As a result, the switching loss becomes significant and the efficiency of the converter reduced sharply. In addition, MHz switching converter exposed to a number of problems existing from passive and active components. For instance, the loss connected with the charging and discharging of the parasitic capacitance, the power MOSFETs becomes significant. The high-frequency behaviour of the devices is very different from the low-frequency behavior. In the design in terms of using passive components, it is important to improve their temperature stability and to minimize the unwanted drift and parasitic elements.

In the design of printed circuit board, it is critical to eliminate undesired coupling between neighboring components. The rest of the circuit, without addressing these issues, the converter does not operate at a high frequency. In the device-level, packaging and circuit interconnection technology has proposed to reduce the structural parasitic and to improve the thermal management. However, the thermal performance and EMI are very hard to solve individually because they are closely related to the circuit layout and packaging. Here inductor–capacitor (LC) series resonant circuit concept has used to perform the PF correction. Problems in Existing System:

1) The existing system is only applicable to linear loads such as resistive load.
2) Switching losses of the power converter is high due to absence of zero comparator PFC stage control.
3) In the existing system, the power factor value is 0.95, which is lower than the proposed system.
4) In the existing system, the Total Harmonics Distortion (THD) present in the input current is 22%, but in the proposed system, it has reduced to 9%.
5) The voltage THD is also higher in the existing system than the proposed system.

III. Block Diagram of Proposed System

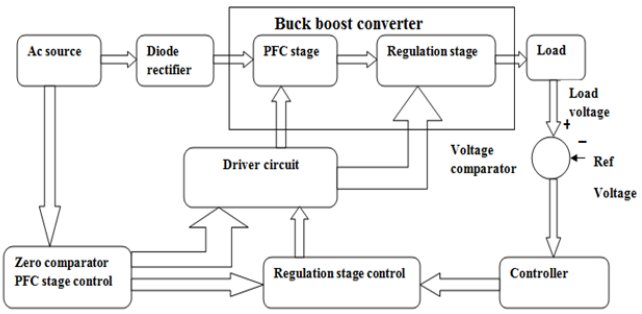

Fig. 4 Block Diagram of Proposed System

The input AC supply has given to the diode rectifier circuit which converts dc supply. The input AC voltage has also given to the zero comparator PFC stage control to generate the control signals of switches in the PFC stage through the driver circuit. The output of the zero comparator PFC stage control is also given to the Regulation stage control. The output of Diode rectifier circuit is given to the PFC stage and Regulation stage which contains power converter i.e. Buck-Boost converter. Regulated output is given to the RL load. The load voltage is sensed and fed to the voltage comparator which compares the actual load voltage with reference voltage and generates the Error signal. The Error voltage is applied to a compensator to generate the threshold voltage V_{cr}min for the resonant capacitors C_{r1} and C_{r2}. The minimum resonant capacitor voltage is applied to the regulation stage control. After that capacitor voltage V_{cr1} and V_{cr2} are being sensed and compared with V_{cr},min to generate the PWM signal for the regulation stage. The operation of power factor correction stage and regulation stage is same as that of existing system. The only difference is that , In existing system the input AC voltage is sensed, and fed to the PFC stage control, instead of PFC stage control Zero Comparator PFC Stage control is used. The Zero comparator PFC stage control has more advantages, because it reduces the THD and increases the input power factor by making the current more sinusoidal than the existing system. The existing system uses the R load and this system is applicable for R load. But the proposed system uses RL load. In the proposed system, the power factor has improved than the existing system, and the current harmonics and voltage harmonics have reduced than the existing system.

IV. Modes of Operation

A. Mode 1 (zero < t < t1):

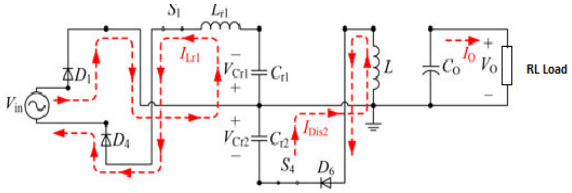

Fig. 5 Equivalent Circuit Diagram of Mode 1

Prior to turning the switches S1 and S4 ON, the capacitor Cr1 and Cr2 are assumed to be charged to V_{cr}min and V_{CR} max, respectively. The positive half-cycle begins at t = 0. In the PFC stage, switch S1, is turned ON, and switch S2, is turned OFF. Diodes D1 and D4 are in the conducting state but diodes D2 and D3 are not conducting state [see Fig 5]. Lr1 and Cr1 have connected in series to form a series resonant circuit. After that, the first half of the resonance takes place and the inductor current starts from an initial value (zero).After that first half of a sinusoidal waveform and then decreases to zero as D1 and D4 block the reverse current flow. Meanwhile, the voltage of capacitor Cr1 has charged from its initial value V_{CR} min to a certain level at t = t1. In the regulation stage, switch S4 has turned ON and diode D6 is in its conducting state. Switch S3 has turned OFF and diodes D5 and D7 are reverse biased. The inductor L is adequately large, so the current I_L has assumed to be a constant magnitude and Capacitor Cr2 and inductor L are formed a closed circuit. The capacitor Cr2 has discharged in one direction due to the polarity of diode D6 up to the voltage of capacitor Cr2 is equal to the minimum voltage (V_{cr}min). The minimum voltage of capacitor Cr2 is either a positive voltage (V_{cr}min > 0), zero voltage (V_{cr}min = 0), or negative voltage (V_{cr}min < 0) depending on the output power. The Energy has transferred from the PFC stage to the regulation stage and that is stored in the inductor L. In this period, the output capacitor C_0, delivers energy to the output load RL.

B. Mode 2(t1<t<t2):

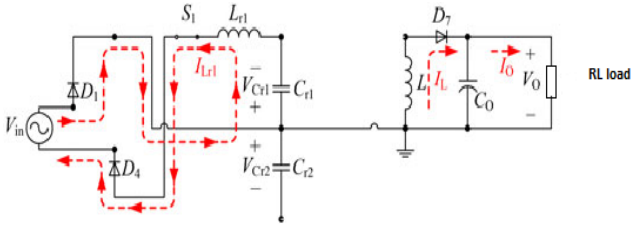

Fig.6 Equivalent Circuit Diagram of Mode 2

In the PFC stage, the functions of the switches (S1 and S2) and the diodes (D1, D2, D3, and D4) are the same as that of Mode 1.Thus, the capacitor Cr1 is kept charging by the power source to the level V_{CR} max, at t = t2. Now, ILr1 becomes zero and the switch S1 has commutated OFF naturally when the diodes D1 and D4 becomes non-conducting state. On the regulation stage, the switch S3 and the diode D5 remains in OFF state, when S4 has turned OFF at t = t1 and D6 is reverse biased when the voltage of Cr2 is equal to V_{cr}min. Now, capacitor Cr2, has not connected to the PFC stage or the regulation stage. The current of an inductor (L) haven't been changed instantaneously, resulting in the forward-biased conduction of diode D7.Therefore, the energy stored in inductor L has delivered to the output capacitor C0 and the load RL.

C. Mode 3 (t2 < t < t3):

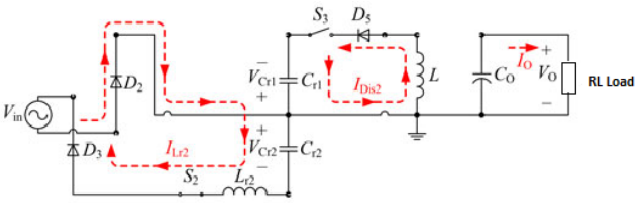

Fig. 7 Equivalent Circuit Diagram of Mode 3

In the negative half-cycle of V_{IN}, the negative parts of the waveforms are similar to that of the positive half-cycle. In the PFC stage, switch S2, is turned ON and switch S1 is turned OFF. Diodes D2, and D3 are in the conducting state while diodes D2 and D3 are reverse biased (see Fig 7). Resonant tank Lr2−Cr2 has connected in series with the input source V_{in} and the input current I_{in} is shaped as a sinusoidal waveform. The voltage on capacitor Cr2 has charged from the initial value V_{cr}min to V_{CR} max. The Energy has transferred from the input source V_{in} to capacitor Cr2. In the regulation stage, the switch S4, and diode D6 remain in the OFF state. Switch S3 has turned ON and the Diode D5 is in the conducting state, while D7 has reverse biased. The energy stored in resonant capacitor C_{rl} that has transferred to inductor L. The C_{rl} has discharged to the inductor L until the voltage of capacitor C_{rl} is equal to V_{cr}min .Similarly to Mode 1, the load RL has supplied by the output capacitor C_0.

D. Mode 4 (t3 < t < ts):

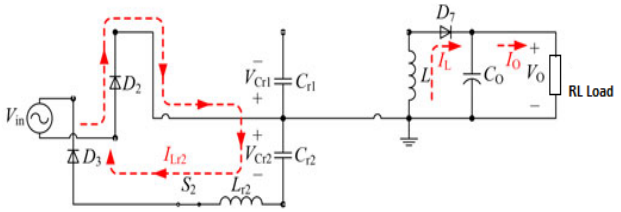

Fig.8 Equivalent Circuit Diagram of Mode 4

In the PFC stage, the conditions of the switches (S1, and S2) and the diodes (D1, D2, D3, and D4) are the same as that of the Mode 3. In the regulation stage, the switch S3 has turned OFF at t = t3,which results the voltage of Cr1 is equal to V_{cr}min. The Energy stored in inductor L has transferred to output capacitor C_0 and load RL through diode D7 and its equivalent circuit diagram has shown in Fig.8. The Switch S2 has commutated OFF naturally when the input source V_{in} becomes positive at t = t_s. Finally, the switches S1 and S4 have turned ON and the positive part of the operation has repeated.

TABLE I
SWITCHING CONDITIONS FOR MODES OF OPERATION

Modes	Time Period	S1	S2	S3	S4
Mode 1	0<t<t1	1	0	0	1
Mode 2	t1<t<t2	1	0	0	0
Mode 3	t2<t<t3	0	1	1	0
Mode 4	t3<t<ts	1	1	0	0

V. Gate Pulse Generation

The gate pulse signal generation for switches S1and S2, S3 and S4 are shown in below figures. Here, four operating modes have been used to get desired voltage and current waveforms for the given circuits. In the PFC stage, the switches S1 and S_2 are used to select the resonant tanks L_{r1}-C_{r1} and L_{r2}-$C_{r2.}$ These resonant tanks have selected corresponding to positive and negative half cycles. In the regulation stage, S4 and S3, are the switches for the controlling the buck- boost converter in the positive and negative half cycles respectively. Here, it is assumed that $C_{r1} = C_{r2}$ and $L_{r1} = L_{r2}$.

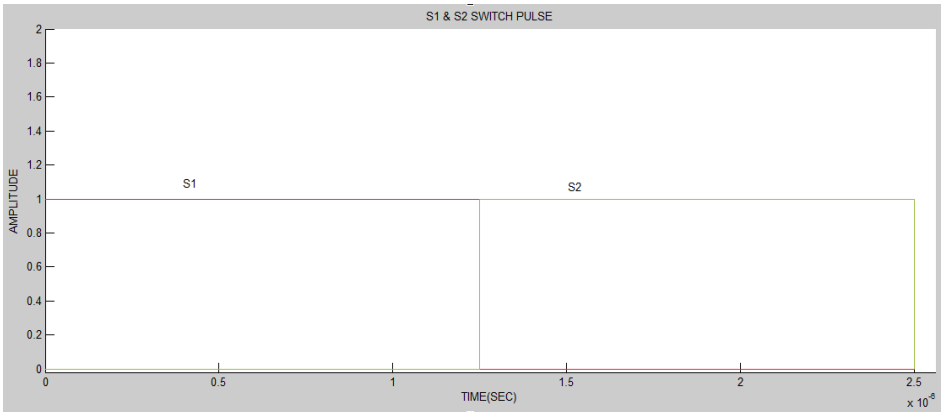

Fig. 9 Gate pulse signals for Switches S1, S2

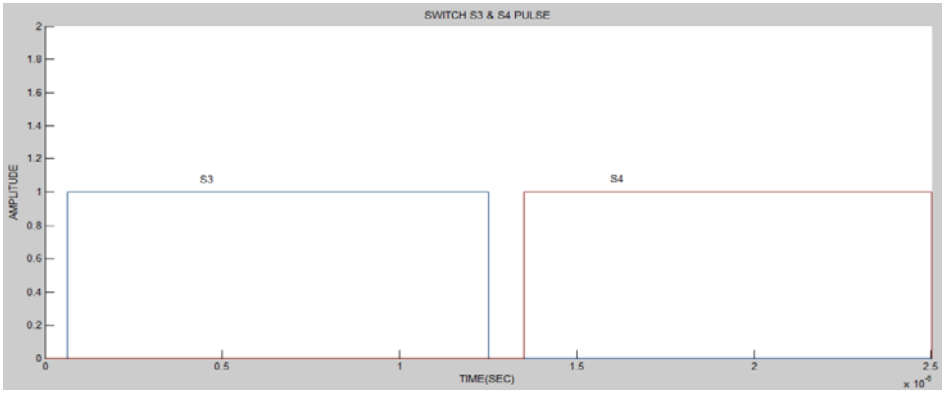

Fig. 10 Gate pulse signals for Switches S3, S4

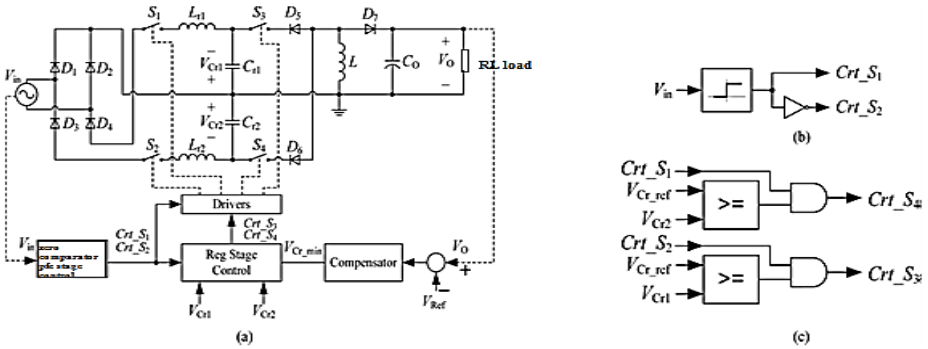

Fig. 11 (a) Overall Control Block Diagram (b) Control Circuit of the PFC Stage (c) Control circuit of the Regulation Stage

VI. Control Methodology

Fig.11 (a) shows the block diagram of the proposed high-frequency AC–DC power converter. On PFC stage, the AC source voltage V_{in} is sensed and fed to a phase detector circuit (Fig 11(b)) .The outputs of the phase detector have connected to the driver circuit to control the ON/OFF time of switches S1 and S2. The signals Crt S1, and Crt S2 are the control signals of switches S1 and S2 respectively. The outputs of the phase detector circuit have also applied to the pulse-width modulation generator to derive the control signals Crt S3 and Crt S4 for switches S3, and S4 respectively.

The load voltage has sensed and fed to the voltage comparator, which compares the actual load voltage with the reference voltage, and generates the error signal. Moreover,

this error signal has applied to the controller to generate the threshold voltage V_{cr}min for the resonant capacitors Cr1 and Cr2. In addition, Fig 11 (c) shows the control circuit of the regulation stage. Here, the instantaneous voltage of the resonant capacitors V_{Cr1} and V_{Cr2} have been sensed and compared with V_{cr}min to generate the pulse width of the switches S3 and S4. The proposed control circuit has been implemented using simple operational amplifiers and digital logic gates. Consequently, it easily fabricated as an Integrated Circuit (IC) for mass production.

VII. MATLAB Simulation Circuit

To verify the operating performance of the proposed converter based controller is simulated using MATLAB software.

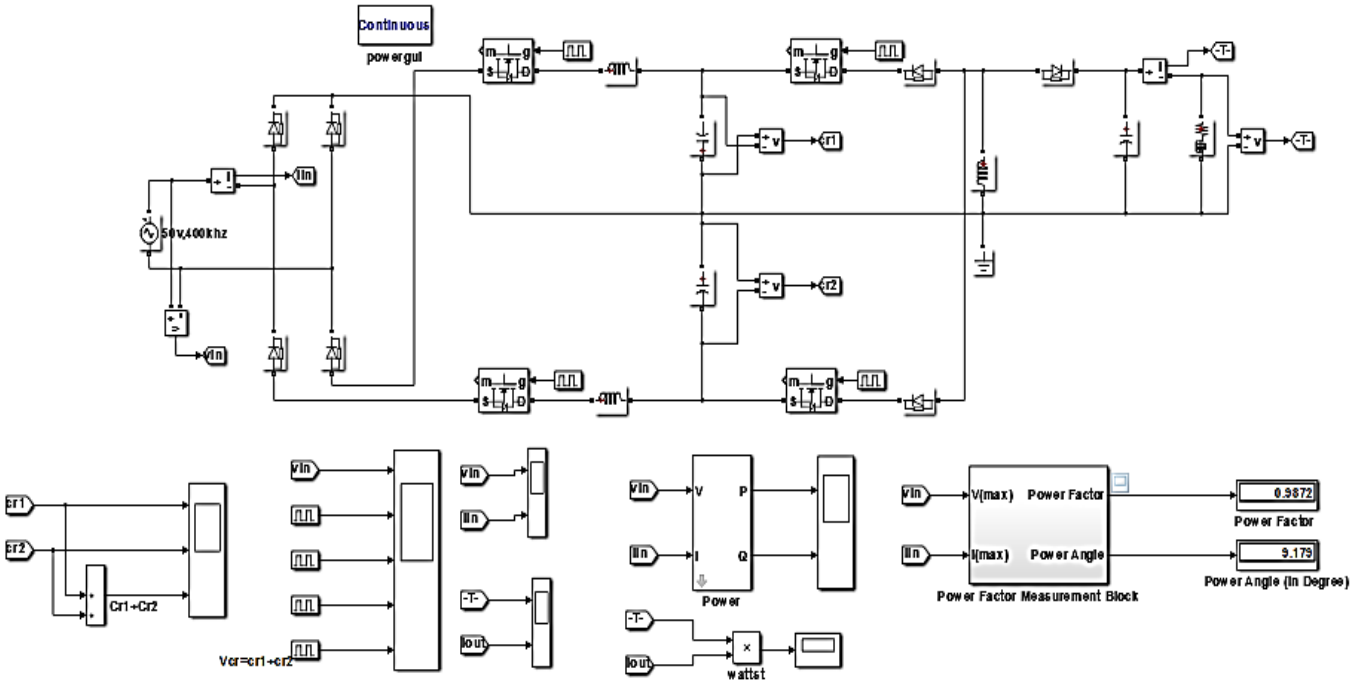

Fig. 12 Proposed Simulation Circuit

VIII .Simulation Results

The following figures show the captured waveforms of input voltage, input current, input power, output voltage, output current and output power of the converter at different level. The output power of the converter is increased from 11 to 30 Watts, when the threshold voltage has reduced from 25 to 50 Volts. In addition, the converter has connected to a constant RL load. Therefore, the output voltage has changed from 29 Volt to 54 Volt accordingly. The experimental waveforms are well in agreement with the theoretical analysis as shown in the below.

E. Input Voltage:

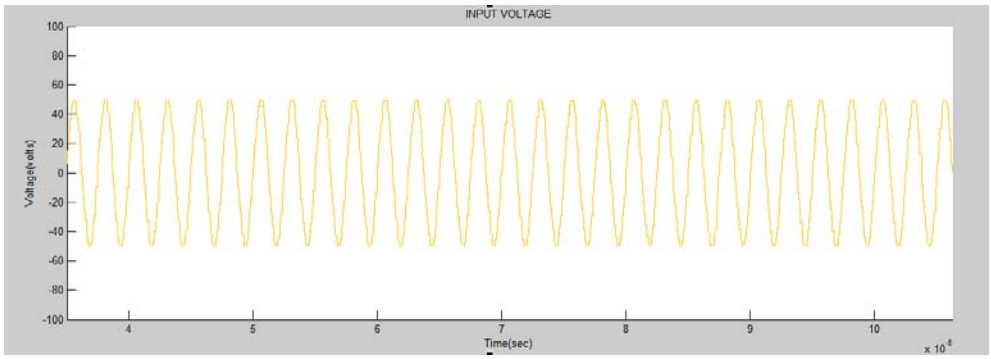

Fig.13 Waveform of input voltage

F. Input Current:

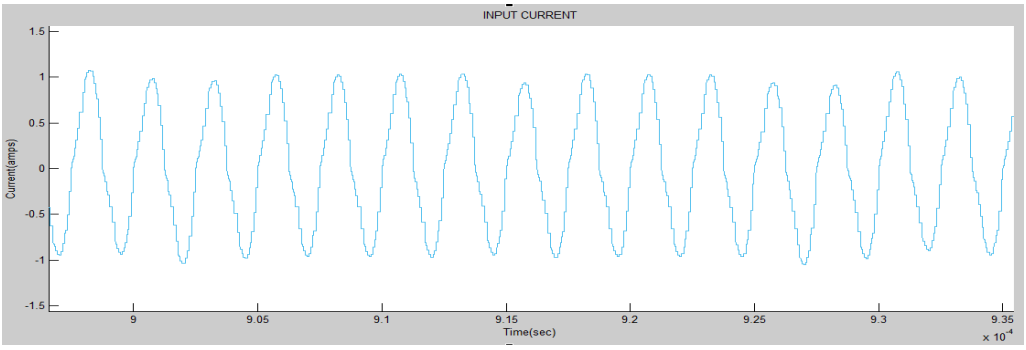

Fig.14 Waveform of input current

G. Input Power:

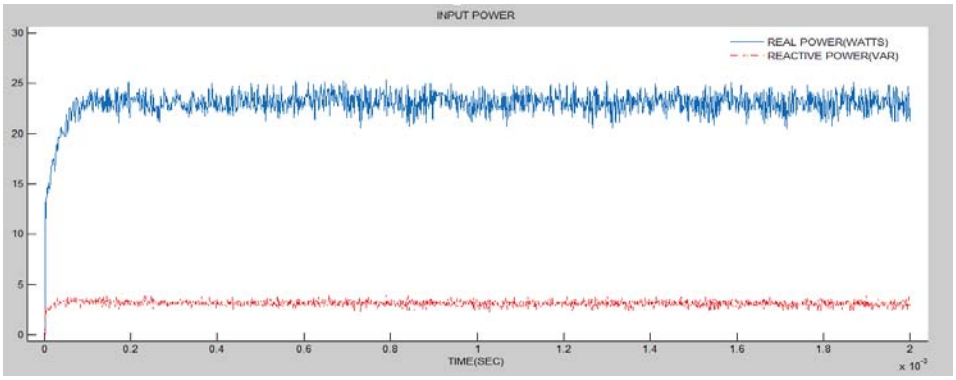

Fig.15 Waveform of input power

H. Output Voltage:

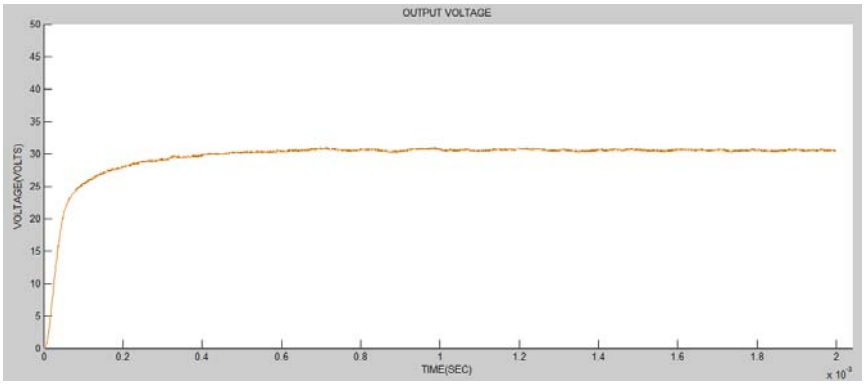

Fig.16 Waveform of output voltage

I. Output Current:

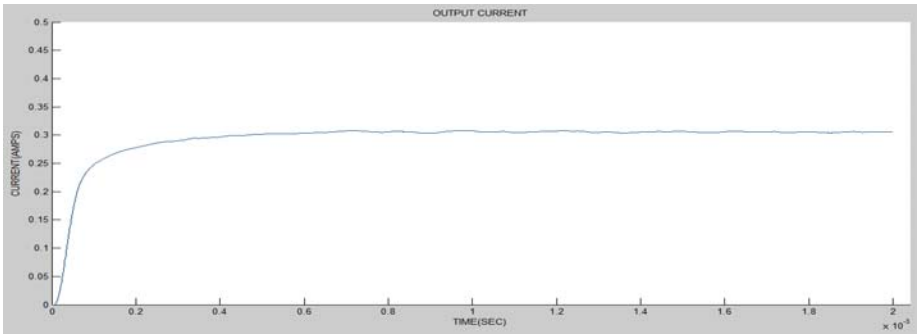

Fig. 17 Waveform of output Current

J. Output Power:

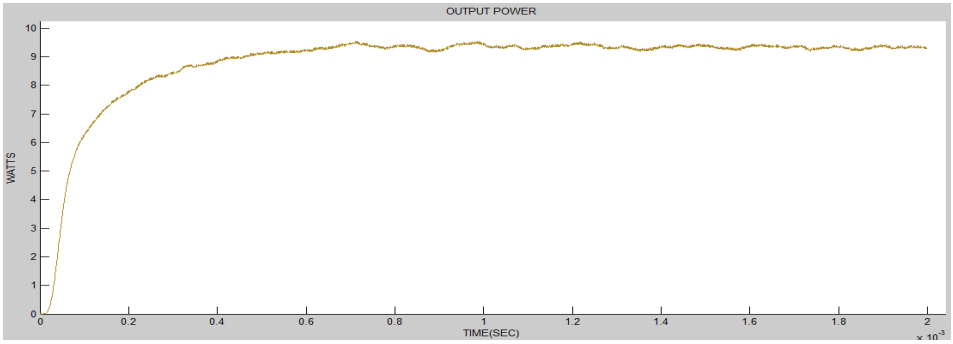

Fig. 18 Waveform of output power

The AC input voltage and current are measured by a digital oscilloscope. Thus, the AC input power of the converter has obtained by integrating the product of the instantaneous input voltage and current. Here, the DC output power measured by the digital multimeter. The PF and overall efficiency of the converter have calculated and the PF of the converter at all the output power levels maintained above 0.9 and the efficiency of the PFC stage, and regulation stage are estimated. They are all within reasonable range from 80% to 90%.The drop of efficiency in the PFC stage has resulted from the high conduction loss of diodes and AC resistance of resonant inductors. The efficiency of the converter has increased based on the selection of components according to the desired applications.

The simplified format shows the Power factor, Current THD, and Voltage THD, which is given in the below.

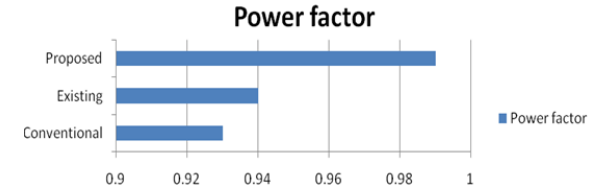

Fig. 19 Value of Power Factor in the Proposed System

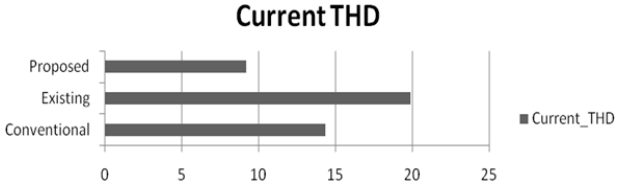

Fig. 20 Value of Current THD in the Proposed System

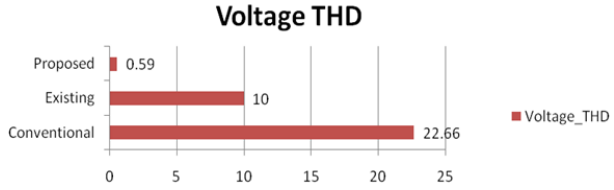

Fig. 21 the Value of Voltage THD in the Proposed System

The detailed studies on the converter design procedure, the passive and active component selection together with the optimization of the voltage conversion ratio and efficiency for practical high-frequency AC-DC applications are available for further work.

IX. Advantages of Proposed System

- ✓ Power factor correction better compares to existing
- ✓ Control the output power
- ✓ Reduced the THD more

TABLE II
COMPARISON BETWEEN EXISTING AND PROPOSED SYSTEM

Parameters	Existing	Proposed
Output power	11.63	10
PF	0.95	0.98
THD	22.66	8

The Output power, Input power is minimized then only our THD will be reduced, and the Power Factor (PF) will be improved.

X. Conclusion

In this system, high switching frequency AC to DC power converter is used for improving the input Power Factor. The Power converter may be Buck-Boost converter, which contains a resonant circuit; with the help of this converter, the efficiency of the power converter is improved. The voltage conversion ratio of the converter can be further controlled by the initial voltage of the resonant capacitors .According to the simulation, the circuit power factor is improved in the range of 0.98 and also the total harmonics distortion (THD < 20%), which is present in the input current is also reduced than the existing system. The distinctive features of this converter are favorable for future high-frequency AC power transfer system operating in the range from a few hundred kHz to the MHz range .The converter operating waveforms are captured to verify the theoretical circuit analysis. The associated input current harmonics and efficiency of the converter are measured.

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