Abstract—In this paper, a CMOS differential operational transresistance amplifier (OTRA) is presented. The amplifier is designed and implemented in a standard umc90-nm CMOS technology. The differential OTRA provides wider bandwidth at high gain. It also shows much better rise and fall time and exhibits a very good input current dynamic range of $-50$ to $50 \mu A$. The OTRA can be used in many analog VLSI applications. The presented amplifier has high gain bandwidth product of $617.6$ THz $\Omega$. The total power dissipation of the presented amplifier is also very low and it is $0.21$ mW.

Keywords—CMOS, differential, operational transresistance amplifier, OTRA, 90 nm, VLSI.

I. INTRODUCTION

The OTRA is generally used in analog VLSI applications. In the past, a great interest has been devoted to the design of the OTRAs [1]-[4]. The bandwidth of a traditional operational amplifier is dependent on the closed loop voltage gain. On the other hand, OTRA is not slew limited like voltage op-amps. It can provide a high bandwidth which is independent of the gain. As a result, it does not suffer from constant gain-bandwidth product as in voltage op-amp circuits [5].

The block diagram of the OTRA is shown in Fig. 1. It is a three terminal analog building block that is defined by the following matrix equation [1]:

$$
\begin{bmatrix}
V_+ \\
V_-
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
R_m & -R_m & 0
\end{bmatrix}
\begin{bmatrix}
I_+ \\
I_-
\end{bmatrix} +
\begin{bmatrix}
0 \\
1
\end{bmatrix} I_o
$$

(1)

where $R_m$ is the transresistance gain.

In the block diagram of the OTRA, the input terminals are virtually grounded, leading to circuits that are insensitive to stray capacitance [6], [7]. The output voltage is the difference of the two input currents multiplied by transresistance $R_m$. Ideally, the transresistance gain $R_m$ approaches infinity and both the input and output terminals are characterized by low impedance. The transresistance gain $R_m$ will apply external negative feedback which force the two input currents $I_+$ and $I_-$ to be equal.

Suppose, all current mirrors are cascode current mirrors, then $R_m$ is given as [8],

$$R_m = \frac{(0.5I_{bias})^2}{(\lambda I_{bias})^2}
$$

(3)

The traditional amplifier shown in Fig. 2 is connected as a non-inverting amplifier, as shown in Fig. 3. The voltage gain is given as

$$\frac{V_o}{V_{in}} = \frac{R_m(\frac{1}{z_1})}{1+R_m(\frac{1}{z_2})}
$$

(4)

If $R_m(\frac{1}{z_2})$ is much greater than 1, then the voltage gain is equal to $\frac{1}{z_2}z_1$, which is the ideal voltage gain $G$. If $R_m$ is represented as $P(s)/Q(s)$, then (3) can be written as [3],

$$\frac{V_o}{V_{in}} = G \frac{P(s)}{P(s) + z_2 Q(s)}
$$

(5)

In order for the poles and zeros of the voltage gain to be the same, $z_2$ must remain same. So, the bandwidth of this circuit is
a constant.

An inverting amplifier is shown in Fig. 4. Its voltage gain is given as,

$$\frac{V_o}{V_{in}} = \frac{R_m \left( \frac{1}{2} \right)}{1 + R_m \left( \frac{2}{2} \right)}$$

(6)

Its bandwidth is also independent of the voltage gain.

III. THE PROPOSED DIFFERENTIAL OTRA

The schematic diagram of the circuit we propose in this paper is shown in Fig. 5. In the proposed high open loop gain differential OTRA, a differential gain stage is used. This low power wide band OTRA is based on a common source amplifier [4] and the cascaded connection of the modified differential current conveyor (MDCC) [6]. The transistors M12-M15 produce the inverting output and the transistors M9-M11 produce the non-inverting output. In the proposed schematic, the DC offset current is reduced and the DC open loop transresistance gain is increased due the addition of the differential gain stage.

If we assume that all the transistors are operating in the saturation region, then the current in the NMOS transistors is given by,

$$I_D = \frac{K}{2} (V_{GS} - V_T)^2$$

(7)

where,

$$K = \mu n C_{ox} \frac{W}{L}$$

(8)

and $V_T$ is the threshold voltage given as,

$$V_T = V_{T_0} + \gamma \left( \sqrt{V_{SB}} + 2 \varphi_f - \sqrt{2 \varphi_f} \right)$$

(9)

The current ($I_B$) in each of the transistors M1, M2 and M3 is equal, because of the current mirrors formed by M4-M6. As a result, the gate to source voltages of M1, M2 and M3 are also equal. Hence, this forces the two input terminals to be virtually grounded. The common source amplifier M15 is used to achieve the high gain, while the transistor pairs (M5 and M6) and (M7 and M8) provide the current differencing operation.
The proposed OTRA has smaller number of current mirrors than the OTRA proposed by Kafrawy and Soliman [1]. As the current mirrors are reduced in the proposed OTRA, this increases the frequency capabilities and also reduces the transistor mirror mismatch effect. Also, the proposed OTRA uses smaller number of transistors when compared with the Kafrawy and Soliman OTRA [1], which reduces the power dissipation.

Consider a single pole model for the transresistance $R_m$, it can be written as,

$$ R_m(s) = \frac{R_o}{1 + \frac{s}{2\pi f_o}} \quad (10) $$

where $f_o$ and $R_o$ are the transresistance cutoff frequency and the DC open loop gain respectively. For high frequency applications, the transresistance gain $R_m(s)$ is expressed as,

$$ R_m(s) \approx \frac{1}{sC_p} \quad (11) $$

where,

$$ C_p = \frac{1}{R_o(2\pi f_o)} \quad (12) $$

IV. ANALYSIS AND VALIDATION RESULTS

The circuit in Fig. 5 is designed and implemented in UMC 1P-9M standard 90-nm CMOS technology. The simulations are carried out in Cadence IC615. Bias settings and transistor dimensions are shown in Table I. The biasing current is $I_B = 29.1 \mu A$ and the biasing voltage is $V_B = -0.9018 \text{V}$. The layout of the circuit is shown in Fig. 6. The circuit occupies an effective area of $79 \times 53 \mu m^2$.

Fig. 7 shows the output voltage of the circuit. This shows an input current dynamic range from $-50 \mu A$ to $50 \mu A$ with the offset current of $0.09 \mu A$.

Fig. 8 shows the frequency characteristics of the open loop transresistance gain of the circuit. The DC open loop transresistance gain here is equal to $182.75 \text{dB} \Omega$ with the gain bandwidth product of $617.6 \text{THz} \Omega$.

![Fig. 6 Layout of the proposed differential OTRA](image)

![Fig. 7 Output voltage (Vo+) of the proposed differential OTRA](image)

![Fig. 8 Frequency characteristics of the open loop transresistance gain for the proposed circuit](image)
TABLE II

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Power Supply (VDD, VSS)</td>
<td>1.5V, -1.5V</td>
<td>1.5V, -1.5V</td>
<td>2.5V, -2.5V</td>
<td>1.5V, -1.5V</td>
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<tr>
<td>No. of Transistors</td>
<td>20</td>
<td>14</td>
<td>17</td>
<td>15</td>
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<td>Total Power dissipation</td>
<td>0.82 mW</td>
<td>0.709 mW</td>
<td>3.96 mW</td>
<td>0.21 mW</td>
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<td>PSRR+</td>
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<td>90.2 dBΩ</td>
<td>NA</td>
<td>198.7 dBΩ</td>
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<tr>
<td>PSRR-</td>
<td>150.1 dBΩ</td>
<td>97.3 dBΩ</td>
<td>NA</td>
<td>163.4 dBΩ</td>
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<td>Input current dynamic range</td>
<td>-50 to 50µA</td>
<td>-50 to 50 µA</td>
<td>-20 to 20µA</td>
<td>-50 to 50µA</td>
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<td>Offset current</td>
<td>0.1 µA</td>
<td>0.3 µA</td>
<td>0.15µA</td>
<td>0.09µA</td>
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<td>DC open loop transresistance gain</td>
<td>163.2 dBΩ</td>
<td>130 dBΩ</td>
<td>4.054dBΩ</td>
<td>182.75dBΩ</td>
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<td>Gain bandwidth product</td>
<td>57.6 THzΩ</td>
<td>3.16 THzΩ</td>
<td>39.8 GHzΩ</td>
<td>617.6THzΩ</td>
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<td>Transresistance gain (-3dB)</td>
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<td>1 MHz</td>
<td>NA</td>
<td>0.45MHz</td>
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<tr>
<td>Rise Time/Fall Time</td>
<td>0.025/1.1 ns</td>
<td>0.023/1.74 ns</td>
<td>NA</td>
<td>0.024/0.97 ns</td>
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</table>

Fig. 9 Transient Response of the proposed circuit

V. CONCLUSION

A modified CMOS differential OTRA is presented. The differential OTRA is designed and implanted in a standard umc90-nm CMOS technology. Simulation results show that the OTRA has high DC open loop transresistance gain and high gain bandwidth product. It also possesses lower offset current and lower power dissipation. A comparison between the proposed differential OTRA and the OTRAs given in [1], [2] and [7] proved the strength of the given circuit.

REFERENCES

