Abstract—In this study, an improved Electrostatic Discharge (ESD) protection circuit with low trigger voltage and high holding voltage is proposed. ESD has become a serious problem in the semiconductor process because the semiconductor density has become very high these days. Therefore, much research has been done to prevent ESD. The proposed circuit is a stacked structure of the new unit structure combined by the Zener Triggering (SCR ZTSCR) and the High Holding Voltage SCR (HHVSCR). The simulation results show that the proposed circuit has low trigger voltage and high holding voltage. And the stack technology is applied to adjust the various operating voltage. As the results, the holding voltage is 7.7 V for 2-stack and 10.7 V for 3-stack.

Keywords—ESD, SCR, latch-up, power clamp, holding voltage.

I. INTRODUCTION

As the device process technology has advanced, the ESD protection circuit is considered as a critical component due to the integrated circuit (IC) failures caused by the heat dissipation [1]. To protect the ICs from the ESD phenomena, the Gate Grounded NMOS (GGNMOS) has mainly been used as an ESD protection circuit. The GGNMOS, however, has the large area and the low current driving capability. It causes a limitation to operating frequency and impedance matching of input-output [2]. On the contrary, Silicon controlled Rectifier (SCR), the other well-known ESD protection circuit, has the high current driving capability and the low area compared to the GGNMOS. It is caused by the positive feedback of the parasitic NPN/PNP bipolar transistors. But the SCR has a trigger voltage of about 20 V and a low holding voltage of about 2 V. The electrical characteristics are vulnerable to the latch-up problem [3]. The latch-up is possible to prevent by the much higher holding voltage. Normally, the holding voltage is only varied by the structural modification [4]-[7].

This paper proposed a stacked circuit with high holding voltage and low trigger voltage. The proposed device is also stacked to get the several fold electrical properties. The simulation was conducted by Synopsys T-CAD simulator.

II. PROPOSED SCR-BASED ESD PROTECTION CIRCUITS

A. The Proposed ESD Protection Circuit

The simple conventional SCR structure is shown in Fig. 1. It consists of the N/P wells and the four diffusion regions. The operation principle of the conventional SCR is as follows.

Fig. 1 A cross section view of conventional SCR
SCR can rapidly discharge the currents to the cathode. The SCR has the structural feature that avalanche breakdown occurs in wide junction region between wells under the surfaces. So, it has a high trigger voltage of about 19V. Also, the holding voltage, which is mainly influenced by the total length and the N-well resistance, is too low to avoid the latch-up [8]. Due to the two electrical properties, the SCR is difficult to design for the ESD protection circuit [9]-[13].

The reasons are as follows. At first, the high trigger voltage has the possibility to cause the damage to the core IC before the protection circuit is triggered under the ESD conditions. Secondly, the holding voltage is too low to prevent the latch-up problem. The holding voltage lower than the operating voltage of the core IC can cause the not-turning-off after discharging the ESD current. Such a latch-up could induce the leakage current and the noise to the input signal. Therefore, the SCRs are not mainly used as the ESD protection circuit in the ICs.

parasitic PNP BJT operating on the surface of the P-well. The PNP BJT has the longer base region than the internal PNP BJT. The longer base region leads to decrease the emitter injection efficiency resulting in reducing the gain (β). Thus, the proposed circuit has the high holding voltage.

Fig. 2 shows a HHVSCR (High Holding Voltage SCR) structure, which is improved from the conventional SCR structure. The structure has the P-drift region on the middle. The operation mechanism of the HHVSCR has the one more

Fig. 2 The cross-sectional view of High Holding Voltage SCR (HHVSCR)

Fig. 3 shows the structure of a Zener Triggering SCR (ZTSCR) with the more improved electrical properties than the HHVSCR. The structural feature of the proposed circuit is the N+ bridge region combined with the P-drift region on the P-Well. The trigger voltage can be much lowered by the breakdown at the highly doped region. Therefore, the proposed circuit has the high holding voltage and the operating principle similar to the SCR due to being based on the HHVSCR. The two circuits have the high holding voltage, which prevents the latch-up. Then, the stack technology, which connects with the same structure sequentially by the previous cathode to the next anode, is applied [14]. The technology is used to take the same advantage of the unit structure though the stack number is increased. By using the stack technology, we proposed the new circuit, which can get the good electrical properties with the trigger voltage and high holding voltage.

Fig. 3 A cross-sectional view of ZTSCR (Zener Triggering SCR)

Fig. 4 A cross-sectional view of the proposed ESD protection circuit
In comparison with the structures, the SCR has the too high trigger voltage and the too low holding voltage to apply the stack technology. For ZTSCR, the trigger voltage is too low. As the stack technology is not ideal method, the stacked ZTSCR can get the lower trigger voltage than the holding voltage, which means the design failure. For HHVSCR, the holding voltage is high enough to avoid the design failures, but the robustness of the HHVSCR can be definitely decreased due to the much higher resistance increase at the drift region. Therefore, in this paper, the newly proposed circuit is used to apply the stack technology for the better electrical characteristics. Fig. 4 shows the newly proposed circuit. The proposed circuit has lower trigger voltage and higher holding voltage than the conventional SCR.

Fig. 5 shows the proposed with applying the stack technology. The structure operates by the ZTSCR operation, and has the very high holding voltage by connecting the two structures.

III. SIMULATION RESULT

A. Analysis of the Proposed ESD Protection Circuit by T-CAD

The simulation was conducted using synopsys’ T-CAD tool to analyze the electrical characteristics. To get the stacked I-V characteristics, the simulations was performed in a mixed mode. The simulated I-V characteristics of ZTSCR and HHVSCR, which is the each single component of the proposed circuits, are shown in Figs. 6 and 7. The numerical values are arranged in Table I.

The simulation results show that the ZTSCR has the trigger voltage of 4.7 V and the holding voltage of 2.2 V, and the HHVSCR has the trigger voltage of 9.7 V and the holding voltage of 2.3 V. The results show that the two structures have the high holding voltages. Fig. 8 and Table II show the simulation results of the electrical characteristics of the conventional SCR and the proposed circuit.
TABLE II  
<table>
<thead>
<tr>
<th>Circuit</th>
<th>Trigger Voltage (Vt)</th>
<th>Holding Voltage (Vh)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional SCR</td>
<td>19.1 V</td>
<td>1.4 V</td>
</tr>
<tr>
<td>Proposed Circuit</td>
<td>16.7 V</td>
<td>3.5 V</td>
</tr>
</tbody>
</table>

Compared to the conventional SCR, the proposed circuit has the lower trigger voltage of 16.7V and the much higher holding voltage of 3.5 V than the SCR. Fig. 9 shows the simulation results of the electrical characteristics as the stack number is increased.

TABLE III  
<table>
<thead>
<tr>
<th>Circuit</th>
<th>Trigger Voltage (Vt)</th>
<th>Holding Voltage (Vh)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed Circuit</td>
<td>16.7 V</td>
<td>3.5 V</td>
</tr>
<tr>
<td>2-Stack</td>
<td>33.5 V</td>
<td>7.7 V</td>
</tr>
<tr>
<td>3-Stack</td>
<td>50.1 V</td>
<td>10.7 V</td>
</tr>
</tbody>
</table>

Therefore, the proposed circuit has the better electrical properties than the conventional SCR.

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