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A Silicon Controlled Rectifier-Based ESD Protection Circuit with High Holding Voltage and High Robustness Characteristics

Kyoung-il Do, Byung-seok Lee, Hee-guk Chae, Jeong-yun Seo Yong-seo Koo

***Abstract*—**In this paper, a Silicon Controlled Rectifier (SCR)-based Electrostatic Discharge (ESD) protection circuit with high holding voltage and high robustness characteristics is proposed. Unlike conventional SCR, the proposed circuit has low trigger voltage and high holding voltage and provides effective ESD protection with latch-up immunity. In addition, the TCAD simulation results show that the proposed circuit has better electrical characteristics than the conventional SCR. A stack technology was used for voltage-specific applications. Consequentially, the proposed circuit has a trigger voltage of 17.60 V and a holding voltage of 3.64 V.

***Keywords*—**ESD, SCR, latch-up, power clamp, holding voltage.

I. Introduction

RECENTLY, with the rapid development of semiconductor integrated circuit technology, the thickness of the gate oxide film of the device unit and the reduction of the metallization line width cause the degradation of the ESD robustness characteristic in the reliability of the integrated circuit (IC). Therefore, ESD has been recognized as an important solution to IC quality and reliability [1]. To solve these ESD problems, researches on electrostatic protection circuits have been conducted. Typical ESD protection circuits to protect IC internal circuit from ESD in semiconductor design and enhance reliability include SCR and Gate Grounded NMOS (GGNMOS). SCR has the advantage of having higher current driving capability than GGNMOS. However, the conventional SCR triggers when the avalanche breakdown in the well, so the trigger voltage is very high, about 19 V. The holding voltage is also very low, about 1 V. A high trigger voltage can damage the oxide of IC, and the low holding voltage can cause latch-up problems. Therefore, the trigger voltage must be lowered to protect the core IC, and the holding voltage must be high to solve the latch-up problem. Generally holding voltage can be increased through structural changes [2]-[5].

In this paper, a SCR-based ESD protection circuit is proposed that compensates for the high trigger voltage and low holding voltage of the SCR. In order to verify the electrical characteristics of the proposed circuit, simulation results were confirmed using Synopsys T-CAD.

Kyoung-il Do, Byung-Seok Lee, Hee-Guk Chae, Jeong-yun Seo are with the Department of Electronics & Electrical Engineering University of Dankook, 126 Jukjeon-dong, Suji-gu, Yongin-si, Gyeonggi-do, 448-701, Korea.

Yong-Seo Koo is with the Department of Electronics & Electrical Engineering University of Dankook, 126 Jukjeon-dong, Suji-gu, Yongin-si, Gyeonggi-do, 448-701, Korea (Corresponding author, e-mail: yskoo@dankook.ac.kr)

II. Proposed SCR-Based ESD Protection Circuits

A. The Proposed ESD Protection Circuit

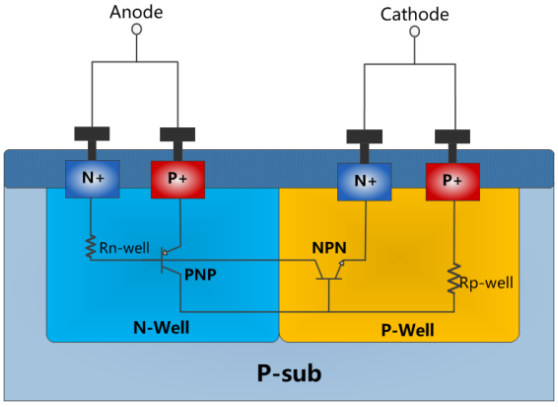

Fig. 1 The cross section view of conventional SCR

Fig. 1 is the cross section of conventional SCR. The structure of conventional SCR consists of P+/N+ diffusion region in N-well, P+/N+ diffusion region in P-well and N/P well. The operation process of SCR is as follows: When the anode voltage increases due to the ESD current flowing from the anode electrode, the left of P+/N+ diffusion region and the N-well voltage rise. Simultaneously, the avalanche breakdown occurs when the electric field between the N-well and the P-well junction in the reverse bias state reaches the threshold value. Electron-hole pairs are generated by the avalanche breakdown phenomenon. The hole current increases the potential of the P-well, so that the P-well and the N+ cathode junction become the forward bias, and the lateral NPN BJT is turned on. The current of the turned-on lateral NPN BJT drops the voltage of the n-well to turn on the lateral PNP BJT. The turn-on currents of the two lateral NPN/PNP BJTs are forwarded by biasing of each base junction to discharge ESD current by latch-up operation [6], [7]. However, due to the high trigger voltage of about 19 V, which is higher than the oxide breakdown voltage, there is a problem that it is difficult to apply the design to the actual IC design area. Latch-up problems can also occur because the holding voltage is very low. Therefore, SCR has many disadvantages to use as an ESD protection circuit [8]-[12].

Fig. 2 is a cross-sectional view of SCR with stack technology. The reason for using the stack technique is for voltage-specific applications. Compared to the conventional stacked SCR, the proposed circuit has higher holding voltage

and latch up immunity.

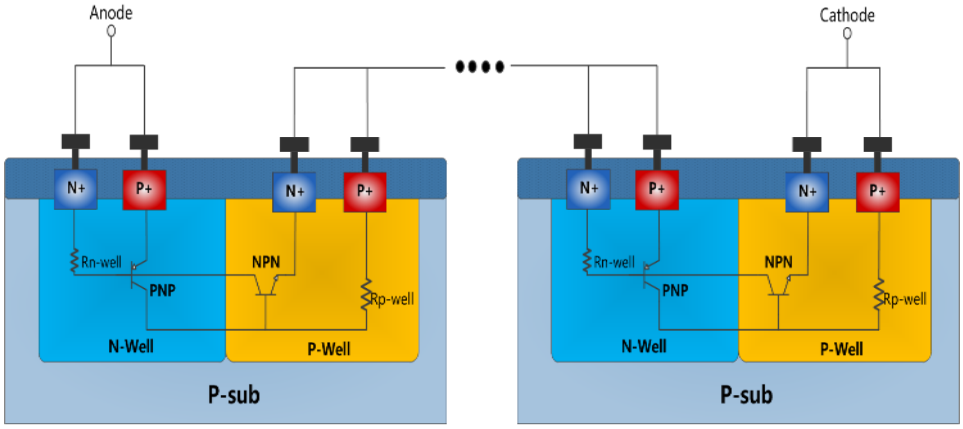

Fig. 2 The cross-sectional view of SCR with stack technology

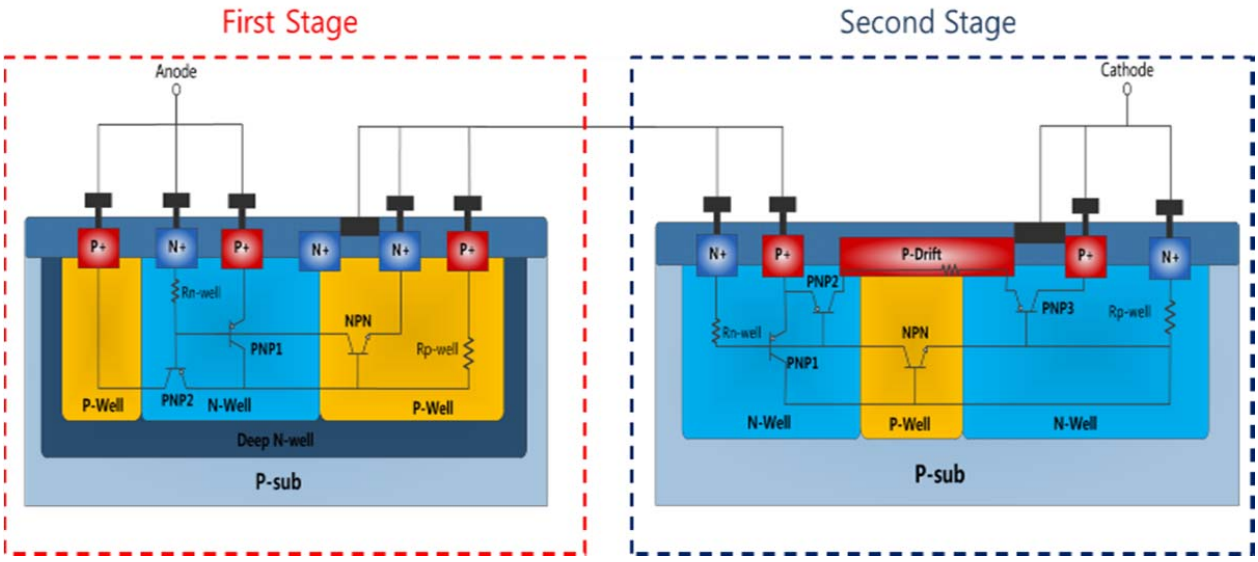

Fig. 3 The cross-sectional view of proposed ESD protection circuit

In this paper, an ESD protection circuit to overcome the disadvantages of conventional SCR is proposed. Fig. 3 is a cross-sectional view of proposed ESD protection circuit. The proposed ESD protection circuit has two parts. The operation principle of the first stage is as follows: In the conventional SCR structure, the avalanche breakdown occurs between the N-well and the P-well. Therefore, the conventional SCR has a high trigger voltage. However, in the case of first stage structure, avalanche breakdown occurs in the N + diffusion region by inserting a GGNMOS. This is the same principle as LVTSCR with low trigger voltage, resulting in a decrease in trigger voltage. In addition, an added parasitic PNP BJT is operated in parallel through P-well and an additional P+ diffusion region in left P-well.

The second PNP BJT forms the other discharge path in parallel reducing on-resistance and improving robustness since the heat is more spread through the additional path.

The second stage is a structure in which a lateral NPN and a PNP transistor are connected as shown in Fig. 3, and the operation principle is as follows: When the ESD pulse is applied to the anode, the potential of the N-well rises, and when the breakdown-threshold voltage between the P-wells is reached, avalanche breakdown occurs and electron-hole pairs are generated. The generated hole current flows to the P-drift and P-well region, thereby increasing the potential of the p-well. As a result, the emitter-base junction of the parasitic NPN bipolar is turned on with a forward bias. Therefore, the current flowing through the parasitic NPN bipolar increases the potential of each N-well to turn on the parasitic PNP bipolar (PNP1, 2 and 3). Each parasitic bipolar performs a latch operation that supplies current to maintain turn-on, so the parasitic PNP/NPN bipolar dissipates the ESD current through the latch operation without further biasing. The second stage of the proposed circuit has good tolerance characteristics because of the operation of four parasitic bipolar transistors.

When applying stack technology to prevent ESD on specific voltage, the ESD design window should be optimized. Because the conventional SCR structure has too high trigger voltage and

low holding voltage, the holding voltage can be increased by using the stacking technique. Therefore, this paper attempts to combine two structures with superior properties. The components of the proposed circuit have high holding voltage, low trigger voltage, and high robustness characteristics. Therefore, the proposed ESD protection circuit, which is a combination of these two, has high holding voltage, low trigger voltage and high robustness characteristics.

III. Simulation Result

A. Analysis of the Proposed ESD Protection Circuit by TCAD SIMULATOR

A synopsys TCAD simulator was used to verify the electrical characteristics of the proposed circuit. For a more accurate electrical comparison, we compare the proposed circuit with the 2-stack of conventional SCR. A comparison of electrical characteristics is shown in Fig. 4 and Table I.

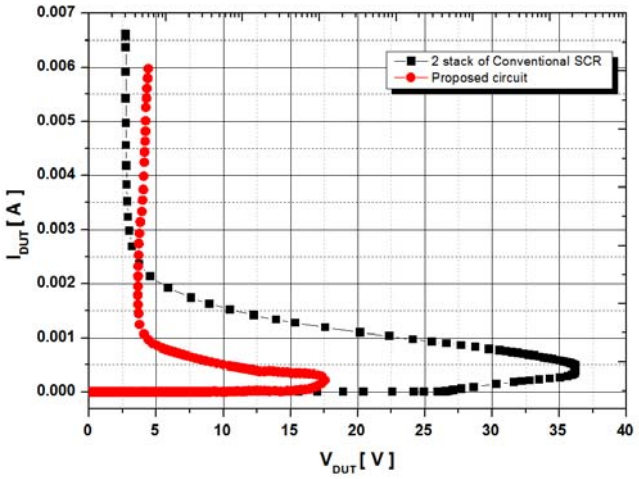

Fig. 4 DC I-V Characteristics curve of the 2-stacked SCR and the proposed circuit

TABLE I
Trigger Voltage and Holding Voltage of the 2-Stacked SCR and Proposed Circuit

Circuit	Trigger Voltage(Vt)	Holding Voltage(Vh)
2-stacked SCR	36.21 V	2.74 V
Proposed Circuit	17.60 V	3.64 V

As shown in Fig. 4 and Table I, the 2-stacked SCR has a high trigger voltage of 36.21V and a low holding voltage of 2.74 V. However, the proposed circuit has much lower trigger voltage of 17.60 V and higher holding voltage of 3.64 V. The proposed circuit has better electrical characteristics than 2-stacked SCR.

Fig. 5 and Table II show the electrical characteristics of the 2-stacked SCR and the circuits fabricated using the stack technology, respectively.

The results of applying the stack technology for voltage-specific applications are shown in Fig. 5 and Table II. Stacked SCRs have trigger voltages of 36.21 V, 72.32 V, and 110.02 V and holding voltages of 2.74 V, 5.49 V, and 8.38 V, respectively. The proposed circuits have trigger voltages of 17.60 V, 33.35 V and 50.96 V and holding voltages of 3.64V, 6.94 V and 10.51 V, respectively. Consequently, the proposed circuit has better electrical properties than 2-stacked SCR.

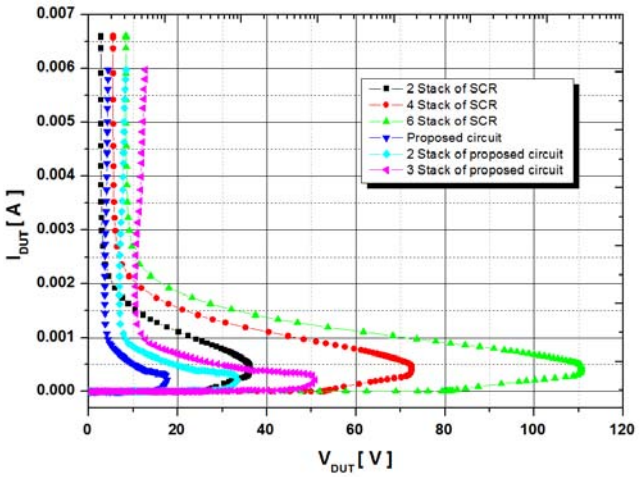

Fig. 5 DC I-V Characteristics curve of the stacked structure of the 2-stacked SCR and the proposed circuit

TABLE II
Trigger Voltage and Holding Voltage of the Stacked Structure of the 2-Stacked SCR and the Proposed Circuit

Circuit	Trigger Voltage(Vt)	Holding Voltage(Vh)
2-Stack of SCR	36.21 V	2.74 V
4-Stack of SCR	72.32 V	5.49 V
6-Stack of SCR	110.02 V	8.38 V
Proposed Circuit	17.60 V	3.64 V
2-stack of Proposed Circuit	33.35 V	6.94 V
4-stack of Proposed Circuit	50.96 V	10.51 V

IV. Conclusion

In this paper, a circuit with a low trigger voltage and a high holding voltage is proposed. In addition, the components of the proposed circuit (first stage, second stage) also have high tolerance characteristics because the parasitic bipolar operates more than conventional SCR. The proposed circuit has a 17.60 V trigger voltage and a holding voltage of 3.64 V. Since the proposed circuit consists of two single circuits, it has better electric characteristics than 2-stack SCR while having similar area to 2-stack SCR. As a result, the proposed circuit has better electrical characteristics than the conventional SCR.

Acknowledgment

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Kyoung-il Do was born in Seoul, Republic of Korea, in 1989. He received the B.S. degrees in electronic engineering from the SeoKyeong University, Seogyeong-ro Seongbuk-gu Seoul, Republic of Korea, in 2016, and is working toward the M.S. degree in electrical and electronics engineering from Dankook University, Yongin-si, Gyeonggi-do, and Republic of Korea. His research interests are the electrostatic discharge (ESD) protection methods and the Power devices.