A Novel Low Power Very Low Voltage High Performance Current Mirror

Khalil Monfaredi, Hassan Faraji Baghtash, Majid Abbasi

Abstract—In this paper a novel high output impedance, low input impedance, wide bandwidth, very simple current mirror with input and output voltage requirements less than that of a simple current mirror is presented. These features are achieved with very simple structure avoiding extra large node impedances to ensure high bandwidth operation.

The circuit’s principle of operation is discussed and compared to simple and low voltage cascode (LVC) current mirrors. Such outstanding features of this current mirror as high output impedance ~384K, low input impedance ~6.4, wide bandwidth ~178MHz, low input voltage ~362mV, low output voltage ~38mV and low current transfer error ~4% (all at 50μA) makes it an outstanding choice for high performance applications. Simulation results in BSIM 0.35μm CMOS technology with HSPICE are given in comparison with simple, and LVC current mirrors to verify and validate the performance of the proposed current mirror.

Keywords— Analog circuits, Current mirror, high frequency, Low power, Low voltage.

I. INTRODUCTION

Current mirror is one of the most essential building blocks in analog integrated circuits which its performance affects qualitative performance of the system. The major draw backs of conventional current mirrors due to technology scaling trend in VLSI design tend to be: voltage supply reduction requirement, input and output impedances degradation, and high frequency malfunctioning. Considering that in many applications, the performance of the traditional current mirrors are inadequate; In the past two decade, a series of high performance current mirrors has been reported [1]-[13]. Low power current mirrors using low supply voltages are attractive for all designers. Meanwhile, traditional current mirrors/sources, such as simple, cascode, and regulated current mirrors/sources [1], suffer from a trade-off between the output resistance and the compliance voltage (the minimum voltage required for the current mirror/source to operate). Some topologies such as the high swing cascaded [2] and the active regulated cascode [3] have improved \( R_{out} \) with a relatively low compliance voltage of \( 2V_{DSsat} \). This, however, may still be too large to be tolerated in low voltage circuits. In [4]-[5] are presented current sources with high output resistance and compliance voltage of one \( V_{DSsat} \). The circuit in [4] works based on sensing the voltage across the current source. Its draw backs are high frequency degradation and instability problems. The circuit in [5] uses positive feedback to increase its output impedance reduce its output compliance voltage. These circuits however are used as current sources and are not suitable as current mirrors. Although the circuits proposed in [6]-[8] eliminate some of the above mentioned draw backs, however they suffer from heavy structures and large chip area consumption. In order to further relaxing voltage requirements some techniques such as body driven topologies are introduced in literatures [9]-[11]. These circuits suffer from lower bandwidth, expensive technology and higher input impedance due to \( g_{mo} \) being lower than \( g_{m} \). Another method for increase the linearity and decrease input voltage swing of current mirrors is to use self biasing structures, which offer reduction in voltage and power supply because of adaptive biasing [13], but they suffer from complexity, larger area. Self biasing improves the performance of current mirrors when the supply voltage is decreased.

In this work a high performance current mirror is presented in which favorably most of aforementioned characteristics are improved.

In section II the proposed current mirror is explained. Section III includes the results achieved from simulations. And finally Section IV concludes this paper.

II. PROPOSED HIGH PERFORMANCE CURRENT MIRROR

A. Principle of Operation

The proposed current mirror, which its schematic is shown in Fig. 1, is composed of M1 and M2 as mirror transistors, M3 and M1p as feedback transistors, M4 as shift transistor, and bias current of \( I_b \). aspect ratio of M4 and I_s are adjusted to set \( V_{ds1} \) equal to \( V_{dcs2} \) prohibiting the channel effect and attaining a high precision result. By using FVF structure [12] at input node low input voltage is achieved and at the same time containing a positive feedback loop of M1, M2, M3, M4, and M1p in the other side causes the input impedance to be extremely low and output impedance to be extremely high. In other words, transistors M2, M4, M3, and M1p create output positive feedback. Transistors M2, M4, M3, and M1 create input positive feedback. The above mentioned positive
feedback in accompany with adaptively biased amplifier M3 in input node preserves low input voltage requirement and low input resistance capability.

Since the loop gain can be controlled by aspect ratios of the transistors hence we can either have negative or positive impedance. This new configuration is capable to operate at output voltages smaller than that of simple current mirror while output compliance no more than that of the simple current mirror is consumed. There is no restriction for transistors M3, M4 and Mp1 to work in saturation region, in fact they can work in saturation, triode, and even off regions. This is an interesting result; firstly because the voltages of circuit are not limited by addition of these transistors, secondly power consumption is not increased very much. For low voltage operation at input node, FVF structure is adopted [12]. This structure makes the circuit to operate at input voltages as low as possible for $V_{D_{sat}}$. It also reduces the input impedance and increases the output impedance.

B. Circuit Analysis

The proposed current mirror is shown in Fig. 1. When the output voltage is increased the channel length modulation effect tends to increase the output current, but meanwhile $W_{UDQVLVWRUV}$ voltage, reducing the M1 and M2 currents. By adjustment of the operating point and aspect ratio of transistors one can achieve very high output impedances even greater than low voltage cascade current mirror while output compliance no more than that of the simple current mirror is consumed. There is no restriction for transistors M3, M4 and Mp1 to work in saturation region, in fact they can work in saturation, triode, and even off regions. This is an interesting result; firstly because the voltages of circuit are not limited by addition of these transistors, secondly power consumption is not increased very much. For low voltage operation at input node, FVF structure is adopted [12]. This structure makes the circuit to operate at input voltages as low as possible for $V_{D_{sat}}$. It also reduces the input impedance and increases the output impedance.

1) Output impedance analysis

Considering small signal equivalent circuit we have:

$$v_{out} = r_{o_2}(I_{out} - g_{m_2}v_{d_3})$$

(1)

$$v_{d_3} = -g_{m_3}r_{p_1}(v_{out} - v_{d_1})$$

(2)

Where:

$$v_{d_1} = -\frac{g_{m_1}}{g_{m_3}}v_{d_3}$$

(3)

Substituting (3) into (2) we get:

$$v_{d_3} = -g_{m_3}r_{p_1}(v_{out} + \frac{g_{m_1}}{g_{m_3}}v_{d_3})$$

(4)

$$v_{d_3} = \frac{-g_{m_3}r_{p_1}(v_{out} + \frac{g_{m_1}}{g_{m_3}}v_{d_3})}{1 + g_{m_1}r_{p_1}(v_{out} + \frac{g_{m_1}}{g_{m_3}}v_{d_3})}$$

(5)

$$v_{d_3} = \frac{-g_{m_3}r_{p_1}(v_{out} + \frac{g_{m_1}}{g_{m_3}}v_{d_3})}{1 + g_{m_1}r_{p_1}(v_{out} + \frac{g_{m_1}}{g_{m_3}}v_{d_3})}$$

(6)

$$v_{d_3} = \frac{-g_{m_3}r_{p_1}(v_{out} + \frac{g_{m_1}}{g_{m_3}}v_{d_3})}{1 + g_{m_1}r_{p_1}(v_{out} + \frac{g_{m_1}}{g_{m_3}}v_{d_3})}$$

(7)

Substituting (7) into (1) gives:
Input impedance analysis

\[
I_{\text{in}} = -g_{m3}(v_{d3} - v_{\text{in}}) + g_{m1}v_{d3}
\]

Where:

\[
v_{d3} = g_{m2}(R_L||r_{\text{d2}})(v_{d3} - v_{\text{in}})
\]

\[
v_{d2} = \frac{g_{m2}(r_{\text{op2}}||r_{\text{d1}})}{g_{m2}(R_L||r_{\text{d2}})}v_{\text{in}}
\]

\[
v_{d3} = \frac{g_{m2}(r_{\text{op2}}||r_{\text{d1}})}{g_{m2}(R_L||r_{\text{d2}})}v_{\text{in}} - \frac{1}{g_{m2}(R_L||r_{\text{d2}})}
\]

By choosing \(g_{\text{out}}\) equal to \(g_{m2}\) we have

\[
I_{\text{in}} = g_{m3}v_{\text{in}} - \left(\frac{1}{(R_L||r_{\text{d2}})}\right)g_{m3}(r_{\text{op2}}||r_{\text{d1}})v_{\text{in}}
\]

\[
R_{\text{in}} = \frac{g_{m3}(r_{\text{op2}}||r_{\text{d1}})}{g_{m3}(r_{\text{op2}}||r_{\text{d1}})} - \frac{1}{g_{m2}(R_L||r_{\text{d2}})}
\]

III. SIMULATION RESULTS

Hspice simulation of the proposed current mirror is carried out in a BSIM 0.35µm CMOS process. To investigate the performance improvement (especially, input and output impedance, input and output voltage swing, power and band width) of the proposed current mirror compared to simple and LVC current mirrors, their simulation results are compared. For a fair judgment the W/L of all investigated circuits is selected the same.

The comparative simulation results are given in Fig. 2 for simple, LVC and proposed circuits. In this figure \(I_{\text{out}}\) is shown in terms of \(V_{\text{out}}\) sweep. It can be seen that the proposed circuits offer higher output impedances and benefit from lower voltage operation capability. Also it can be seen that low voltage cascode exhibits more offset error and does not operate at low voltages. However, low voltage cascode provides higher output impedance compared to proposed current mirror. The proposed current mirror’s well functionality as a low voltage and high resistance block especially at low current levels is comprehensively understood from the Fig.2.

![Fig. 2 comparative simulation results for simple, LVC and proposed circuits](image-url)

**Fig. 2**

**Fig. 3** shows the output current dynamic range for simple, LVC and proposed circuits.

![Fig. 3: output current dynamic range](image-url)

**Fig. 3**

**Fig. 4** compares the input resistance of simple, LVC, and proposed current mirrors.

![Fig. 4](image-url)

**Fig. 4**

By choosing \(g_{\text{out}}\) equal to \(g_{m2}\) we have

\[
I_{\text{in}} = g_{m3}v_{\text{in}} - \left(\frac{1}{(R_L||r_{\text{d2}})}\right)g_{m3}(r_{\text{op2}}||r_{\text{d1}})v_{\text{in}}
\]

\[
R_{\text{in}} = \frac{g_{m3}(r_{\text{op2}}||r_{\text{d1}})}{g_{m3}(r_{\text{op2}}||r_{\text{d1}})} - \frac{1}{g_{m2}(R_L||r_{\text{d2}})}
\]
Fig. 4 The input resistance of simple, LVC, and proposed current mirrors.

Fig. 5 shows the band width of simple, LVC, and proposed current mirror. It is seen that the proposed current mirrors have the high band width of the simple current mirror.

Comparative results of proposed current mirrors with some other works are presented at Table 1.

IV. CONCLUSION

In this work a high performance current mirror is presented with such favorable characteristics as: high output impedance~384K, low input impedance~6.4, wide bandwidth~178MHz, low input voltage ~ 362mV, low output voltage ~ 38mV and low current transfer error ~4% (all at 50µA). Its simulation results in BSIM 0.35µm CMOS technology with Hspice are given in comparison with those of simple, and LVC current mirrors to verify and validate the performance of the proposed current mirror.

The proposed current mirror (CM) shows output impedance greater than traditional cascode current mirrors, while maintaining the output voltage requirement and high bandwidth of the simple current mirror. This circuit’s bandwidth, input and output voltage requirements are comparable to those of the simple current mirror. The circuit can show a minimum output voltage even lower than that of the simple current mirror. The proposed current mirror is an outstanding choice for high frequency low power low voltage applications.

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REFERENCES

Khalil Monfaredi was born in Miyandoab, Azarbajane Gharbi, Iran, in 1979. He received the B.Sc. and M.Sc. degrees from Tabriz University in 2001 and Iran University of Science and Technology in 2003, respectively. He is currently pursuing his Ph.D. degree in Iran University of Science and Technology, Electrical and Electronic Engineering Department. He is with Electronic Research Center Group, since 2001 and is also an academic staff of Islamic Azad University, Miyandoab Branch since 2006. He serves as the Research and Educational Assistant of Miyandoab Sama College since 2009. He is the author or coauthor of more than twenty national and international papers and also collaborated in several research projects. His current research interests include current mode integrated circuit design, low voltage, low power circuit and systems and analog microelectronics and data converters.

Hassan Faraji Baghtash was born in Miyandoab, Iran, in 1985. He received the B.Sc. and M.Sc. degrees from Urmia University in 2007 and Iran University of Science and Technology in 2009, respectively. He is the author or coauthor of more than ten national and international papers and also collaborated in several research projects. He is with Electronic Research Center Group, since 2007 and cooperates with Islamic Azad University-Miyandoab Branch, West Tehran Branch and also Miyandoab Sama Colledge since 2008. He is currently pursuing his Ph.D. degree in Iran University of Science and Technology, Electrical and Electronic Engineering Department. His current research interests include current mode integrated circuit design, low voltage, low power circuit and systems and analog microelectronics and RF design.

Majid Abbasi was born in Abhar, Iran, in 1983. He received the B.Sc. and M.Sc. degrees from Islamic Azad University of Lahijan in 2006 and Iran University of Science and Technology in 2010, respectively. He cooperated with Islamic Azad University-West Tehran Branch since 2010. His current research interests include power electronics and analog microelectronics.