A Low-Voltage Tunable Channel Selection Filter for WiMAX Applications

Kayvan Ahmadi, Hossein Shamsi

Abstract—This paper proposes a low-voltage and low-power fully integrated digitally tuned continuous-time channel selection filter for WiMAX applications. A 5th-order elliptic low-pass filter is realized in a Gm-C topology. The bandwidth of the fully differential filter is reconfigurable from 2.5MHz to 20MHz (8x) for different requirements in WiMAX applications. The filter is simulated in a standard 90nm CMOS process. Simulation results show the THD (@Vout =100mVpp) is less than -66dB. The in-band ripple of the filter is about 0.15dB. The filter consumes 1.5mW from a supply voltage of 0.9V.

Keywords—Common-mode feedback, continuous-time, fully differential transconductor, Gm-C topology, low-voltage

I. INTRODUCTION

WORLDWIDE Interoperability for Microwave Access (WiMAX) technology, according to IEEE 802.16 standards, attracts people's attention recently. It provides fixed, nomadic, portable, and mobile wireless broadband connectivity no matter in a Line-of-Sight (LOS) or Non-Line-of-Sight (NLOS) environment. WiMAX can theoretically support data rate up to 70Mb/s and maximum coverage of 50km. The channel bandwidth is adjustable from 1.25MHz to 20MHz. Therefore, a channel selection filter with variable bandwidth is required for WiMAX applications [1]. Direct conversion architecture is appropriate for these systems because it does not need IF-SAW channel selection filters and subsequent down-conversion stages which are replaced with low-pass filters (LPFs) and baseband amplifiers [2]. In particular, Gm-C tuning is a fairly popular method because of it's potential benefits of high speed and low-power. They have recently received great interest since they are suitable for integration and can operate at high frequencies. Although on-chip active filters consume power, chip area, and limit the overall dynamic range, they enable high integration and bandwidth tuning. Therefore, the design of highly linear and tunable transconductors has become mandatory. In these filters, a fully differential transconductor circuit provides a suitable transconductance value. To achieve a variable bandwidth in Gm-C filters, either the transconductance or the capacitance is held constant while the other is tuned. In this work, all of the transconductors have a constant transconductance and all of the capacitors can vary to achieve the desired cutoff frequencies.

Fig. 1 (a) fully differential source degenerated transconductor, (b) the half circuit of the transconductor

II. FULLY DIFFERENTIAL SOURCE DEGENERATED TRANSCONDUCTOR

In new technology CMOS processes, short channel effects aren’t negligible. They damage the linearity of the circuits. Making use of the fully differential circuits gives better performances in noise, linearity and etc compared with the single ended circuits. Thus, we have to use a fully differential transconductor to achieve better performances [3]-[4]. In an ideal transconductor, the output current is proportional to the input voltage. The relation is shown in (1).

\[ I_{out} = G_m V_{in} \]  

where \( I_{out} \) is the output current and \( V_{in} \) is the input voltage of the transconductor. The parameter \( G_m \) is a constant coefficient that denotes the transconductance value of the transconductor. In an ideal transconductor, the value of \( G_m \) is independent from the amplitude and frequency of the input signal.

Fig. 1 (a) shows a fully differential constant-Gm source degenerated transconductor. All of its transistors operate in the saturation region. M3 and M4 operate as two current sources and M5 and M6 operate as two current sinks. M1 and M2 and resistor \( R_N \) convert the differential input voltage to the differential output current. In order to have a balanced...
circuit, the size of transistors M1, M3 and M5 are chosen identical to that of M2, M4 and M6, respectively.

The transconductor operates as follows: The bias current through both branches of the transconductor is fixed by pMOS transistors M3 and M4. Whenever the differential input signal is zero, the currents of both branches of the transconductor are equal. When the input signal is applied to the gate of M1 and M2, the currents of both branches become different because the input transistors M1 and M2 translate the input voltage to the degeneration resistor. The resistor current is then steered to the high impedance output nodes. This degenerated device is used to provide \( V \) to \( I \) conversion with high linearity. The main reasons of the distortion of the transconductor are the input transistors M1 and M2 and the implementation of the degeneration resistor [5]. The best choice for improving the linearity is to employ a passive source de-

The half circuit of the transconductor is shown in Fig. 1 (b) where \( I_{at} = V_{at} \) is the input differential voltage of the transconductor. The output current of the transconductor is

\[
I_{out} = -g_m v_{gs2}
\]

where \( g_m \) is the transconductance of the transistor M2 and \( v_{gs2} \) is its gate-to-source small signal voltage. So, we have

\[
v_{gs2} = v_{gs} - v_{ds} = -\frac{V_d}{2} - \left( -\frac{R I_{at}}{2} \right)
\]

where \( v_{gs} \) and \( v_{ds} \) are the gate voltage and the source voltage of the transistor M2, respectively. From (1)-(3), we have

\[
\frac{I_{at}}{V_d} = \frac{1}{2} \frac{g_m}{1 + g_m R_s / 2}
\]

Similar to \( I_{at} \), we have

\[
\frac{I_{out}}{V_d} = \frac{1}{2} \frac{g_m}{1 + g_m R_s / 2}
\]

where \( g_m \) is the transconductance of the transistor M1. From (4) and (5) and assuming \( g_m = g_m \), the transconductance value of the transconductor is obtained as follows:

\[
g_m = \frac{I_{out}}{V_{at}} = \frac{V_{gs} - V_{ds}}{V_{at} - V_{ds}} = \frac{g_m}{1 + g_m R_s / 2}
\]

where the \( (I_{out} - I_{at}) \) is the output differential current and the \( (V_{gs} - V_{ds}) \) is the input differential voltage.

The above fully differential circuit needs a common-mode feedback (CMFB) circuit to stabilize the output DC voltage level of the transconductor according to a reference voltage \( V_{\text{REF}} \) [6]. \( V_{\text{CMFB}} \) is generated by a CMFB circuit to set the output DC level of the transconductor. Fig. 2 shows a low-voltage continuous-time CMFB circuit. The output of the op-amp is applied to the circuit of Fig. 1 at node \( V_{\text{CMFB}} \). The nodes \( out^- \) and \( out^+ \) have to be connected to the nodes \( out^- \) and \( out^+ \) in Fig. 1, respectively [6]. The source voltages of the transistors M9 \( (V_{at}) \) and M10 \( (V_{at}) \) are

\[
V_{at} = V_{at} - V_{gs} - V_{gs}
\]

\[
V_{at} = V_{at} - V_{gs} - V_{gs}
\]

and the voltage of node CM \( (V_{CM}) \) is

\[
V_{CM} = V_{at} - RI_x
\]

where \( I_x \) is the current of resistor \( R \) which is

\[
I_x = \frac{V_{at} - V_{at}}{2R}
\]

from (5)-(8), the \( V_{CM} \) is obtained as follows:

\[
V_{CM} = V_{CM1} + V_{CM2}
\]

\[
V_{CM1} = -\frac{V_{gs} + V_{gs} + V_{gs} + V_{gs}}{2}
\]

\[
V_{CM2} = \frac{V_{gs} + V_{gs}}{2}
\]

The voltage of node CM consists of two terms \( V_{CM1} \) and \( V_{CM2} \) that the first term \( V_{CM1} \) is independent from the voltage of nodes \( out^- \) and \( out^+ \). It is only dependent on bias currents of M7, M8, M9 and M10. The second term \( V_{CM2} \) is only dependent on the common-mode voltage of nodes \( out^- \) and \( out^+ \). When the output DC voltage level of the transconductor increases, the voltage of the node CM increases, too. The op-amp compares the increased common-mode voltage with the reference voltage which is applied to the op-amp \( (V_{\text{REF}}) \) and increases the voltage \( V_{\text{CMFB}} \). Increasing the voltage \( V_{\text{CMFB}} \) causes decreasing the output DC voltage level of the transconductor of Fig. 1. This means that the CMFB circuit has a negative feedback. If

\[
V_{\text{REF}} = V_{CM1} + V_{\text{desired}}
\]

The CMFB circuit sets the output DC voltage level to the voltage \( V_{\text{desired}} \).

Fig. 3 shows the simple op-amp used in CMFB circuit. It is a differential amplifier with an active load to have high voltage gain.
III. 5th-order Elliptic LPF Design

A. Filter Design

The main characteristic of an elliptic filter is its sharp magnitude response compared with the other filters such as Butterworth, Bessel and etc. The biquad circuit realization for the filter is used because of its advantages in design and layout. Furthermore, this approach compared to the ladder filters has the advantage that the filter is not a single complicated structure but the cascade of simple blocks. A disadvantage of the biquad filters compared to the ladder filters has the larger sensitivity to the component variations [7].

The normalized \((\omega_0 = 1)\) transfer function of the 5th-order elliptic filter is

\[
H(S) = H_1(S) \cdot H_2(S) \cdot H_3(S)\]

(15)

where the \(H_1, H_2\) and \(H_3\) are

\[
H_1(S) = \frac{0.043S^2 + 0.36}{S^2 + 0.77S + 0.52}
\]

(16)

\[
H_2(S) = \frac{0.043S^2 + 0.92}{S^2 + 0.28S + 0.94}
\]

(17)

\[
H_3(S) = 0.73 \left(\frac{S}{S + 0.50}\right)
\]

(18)

Fig. 4 shows a 5th-order elliptic low-pass filter. The filter is made by four cascaded blocks. The first block \(H_1\) is a biquad filter with two zeroes and the second block is a fully differential unity gain amplifier. The third block \(H_2\) is a biquad filter with two zeroes and the last block \(H_3\) is a 1st-order filter without any zero [2]. The transfer function of the biquad Gm-C filters (\(H_1\) and \(H_2\)) is

\[
H(S) = \frac{K_2S^2 + K_1S + K_0}{S^2 + \left(\frac{\omega_0}{Q}\right)S + \omega_0^2}
\]

(19)

\[
K_1 = \left(\frac{C_i}{C_i + C_0}\right) \quad K_2 = \left(\frac{G_{m1}}{C_i(C_i + C_0)}\right)
\]

(20)

where the transfer function of the 1st-order low-pass Gm-C filter (\(H_3\)) is

\[
H_3(S) = \frac{G_{m2}}{S + G_{m1}}
\]

(21)

From (13)-(15), the desired transconductance values of the
Gm-C filter are obtained as shown in Table I. In order to avoid loading effects of block \( H_2 \) on block \( H_1 \), a fully differential amplifier with high input impedance and low output impedance is placed between them. This amplifier is shown in Fig. 5. The amplifier is made by a differential pair with diode connected load transistors.

**B. Cutoff Frequency Tuning**

By varying the capacitors, the corner frequency of the filter will change. Fig. 6 shows a 2-bits digitally tuned capacitor array [7]. Table II shows the relation between input control bits status and total equivalent capacitance of the array. When a control bit goes to ‘1’, the MOS transistor which is connected to the control bit, goes to triode region and the total capacitance of the capacitor array increases. If all of the control bits are ‘0’, the capacitance of the variable capacitor has its lowest value that gives the maximum cutoff frequency. When two control bits are ‘1’, the capacitance of the variable capacitor has its highest value that gives the minimum cutoff frequency of the filter. The desired capacitance values of the capacitor array are shown in Table III.

**TABLE I**

<table>
<thead>
<tr>
<th>( G_{m1} )</th>
<th>( G_{m2} )</th>
<th>( G_{m3} )</th>
<th>( G_{m4} )</th>
<th>( G_{m5} )</th>
<th>( G_{m6} )</th>
<th>( G_{m7} )</th>
<th>( G_{m8} )</th>
<th>( G_{m9} )</th>
<th>( G_{m10} )</th>
<th>( G_{m11} )</th>
<th>( G_{m12} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>37.6µS</td>
<td>35.5µS</td>
<td>0</td>
<td>0</td>
<td>54.2µS</td>
<td>71.4µS</td>
<td>72.6µS</td>
<td>59.2µS</td>
<td>54.5µS</td>
<td>21.2µS</td>
<td>54.5µS</td>
<td>37.2µS</td>
</tr>
</tbody>
</table>

**TABLE II**

<table>
<thead>
<tr>
<th>‘( V_d1 ) \ V_d0 \’</th>
<th>( C_{equivalent} )</th>
<th>Cutoff freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>( C_4 )</td>
<td>20MHz</td>
</tr>
<tr>
<td>01</td>
<td>( C_4+C_2 )</td>
<td>10MHz</td>
</tr>
<tr>
<td>10</td>
<td>( C_4+C_1 )</td>
<td>5MHz</td>
</tr>
<tr>
<td>11</td>
<td>( C_4+C_2+C_1+C_3 )</td>
<td>2.5MHz</td>
</tr>
</tbody>
</table>

**TABLE III**

<table>
<thead>
<tr>
<th>( C_a )</th>
<th>( C_b )</th>
<th>( C_x )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_1 )</td>
<td>3.3 pF</td>
<td>3.6pF</td>
</tr>
<tr>
<td>( C_2 )</td>
<td>1.1pF</td>
<td>1.1pF</td>
</tr>
<tr>
<td>( C_3 )</td>
<td>3.6 pF</td>
<td>3.42pF</td>
</tr>
<tr>
<td>( C_4 )</td>
<td>1.2pF</td>
<td>1.1pF</td>
</tr>
</tbody>
</table>

**IV. SIMULATION RESULTS**

Making use of the described fully differential transconductor, the above 5th-order elliptic LPF is simulated with HSPICE in a 90nm CMOS technology. The supply voltage of the filter is 0.9V. Fig. 7 shows the differential output current of the transconductor \( I_{out} = I_{var} \) versus the differential input voltage of the transconductor. Fig. 8 shows the simulated large signal transconductance value of the transconductor as a function of the differential input voltage, where \( R_N \) varies from 5k\( \Omega \) to 24k\( \Omega \). The frequency response of the normalized transconductance \( G_m/G_m0 \) is depicted in Fig. 9. In this simulation we have: \( G_m0=35\mu S \). In Fig. 10 the frequency response of the filter is shown. In order to achieve the required tuning range, capacitors are switched so that the cutoff frequencies (fc) are tuned from 2.5MHz to 20MHz corresponding to the digital tuning inputs. In Fig. 11 the THD of the output voltage of the filter versus the peak-to-peak amplitude of the input signal of the filter is depicted. Table IV summarizes the simulation results of the filter.

**V. CONCLUSIONS**

A fully differential, fully integrated, low-voltage, and low-power Gm-C filter has been simulated in a standard 90nm CMOS process. To avoid the short channel effects, the filter has been made by using a fully differential constant-Gm transconductor. The filter consumes 1.5mW from a supply voltage of 0.9V. The corner frequency of the filter can be adjusted between 2.5MHz and 20MHz by applying 2-bits digital inputs.
Fig. 7 The differential output current of the transconductor versus its differential input voltage.

Fig. 8 Transconductance (Gm) versus the differential input voltage of the transconductor.

Fig. 9 Normalized transconductance (Gm/Gm0) frequency response (Gm0=35µS).

Fig. 10 Magnitude response of the filter.

Fig. 11 THD versus input voltage of the filter.

### Table IV

<table>
<thead>
<tr>
<th>Technology</th>
<th>90nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>0.9V</td>
</tr>
<tr>
<td>Filter type</td>
<td>5th-order elliptic</td>
</tr>
<tr>
<td>Tuning range of fc</td>
<td>2.5MHz–20MHz (8x)</td>
</tr>
<tr>
<td>In-band ripple</td>
<td>0.15dB</td>
</tr>
<tr>
<td>Total input eq. noise</td>
<td>462µVrms</td>
</tr>
<tr>
<td>THD (@Vout=100mVpp)</td>
<td>-66dB</td>
</tr>
<tr>
<td>Att. (@fstop=4×fc)</td>
<td>79dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.5mW</td>
</tr>
</tbody>
</table>

### REFERENCES


