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20 GHz Fractional Phased Locked Loop Circuit for the Gbps Wireless Communication

Ki-Jin Kim, Sanghoon Park, and K. H. Ahn

***Abstract*—**This paper presents the 20-GHz fractional PLL (Phase Locked Loop) circuit for the next generation Wi-Fi by using 90 nm TSMC process. The newly suggested millimeter wave 16/17 pre-scalar is designed and verified by measurement to make the fractional PLL having a low quantization noise. The operational bandwidth of the 60 GHz system is 15 % of the carrier frequency which requires large value of Kv (VCO control gain) resulting in degradation of phase noise. To solve this problem, this paper adopts AFC (Automatic Frequency Controller) controlled 4-bit millimeter wave VCO with small value of Kv. Also constant Kv is implemented using 4-bit varactor bank. The measured operational bandwidth is 18.2 ~ 23.2 GHz which is 25 % of the carrier frequency. The phase noise of -58 and -96.2 dBc/Hz at 100 KHz and 1 MHz offset is measured respectively. The total power consumption of the PLL is only 30 mW.

***Keywords*—**Millimeter Wave Fractional PLL, Wide band VCO, WPAN Transceiver.

I. Introduction

THE 57-66 GHz band has been allocated for high dara WPAN (Wireless Personal Area Network), wireless HD and next generation Gbps Wi-Fi. As defined by IEEE 802.15.3c and 802.11ad standards, four channels of 2.16 GHz bandwidth are allocated for 7 Gbps communication in 16 QAM (Quadrature Amplitude Modulation). However, it is still challenging work to realize 16-QAM communication in 60 GHz mainly due to performance of the PLL phase noise. The required phase noise for 16-QAM was reported in previous study [1]. It showed that the phase noise of below -90 dBc/Hz at 1 MHz offset is required for ignoring BER degradation from phase noise of the PLL.

Previously reported CMOS PLLs were mainly integer type synthesizers [2], [3] because it is difficult to realize the pre-scalar at the millimetre wave frequency. The integer PLL is limited in usage because the output frequency of the PLL is defined to integer multiple value of the TCXO (Temperature Compensated Crystal Oscillator). Acording to the ECMA standard, the channel bonding which combines two or four channels of 2.16 GHz band is introduced. Considering channel bonding requiring fractional frequency generation, a millimeter waver fractional PLL is imperative in future 60 GHz system.

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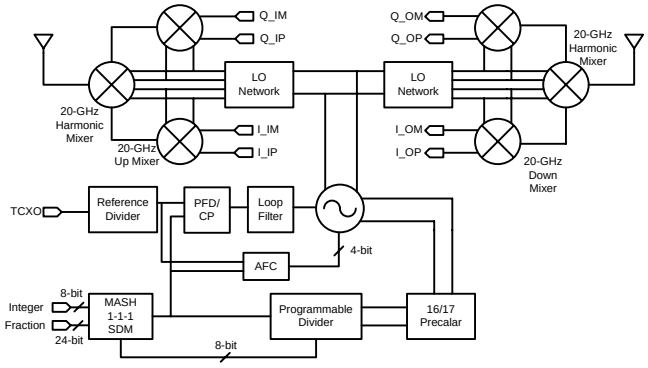

Fig. 1 Block diagram of the PLL and transceiver architecture

This paper presents the 20-GHz fractional PLL with 4-bit controlled VCO. The reason why the 20 GHz is chosen for 60 GHz system is illustrated in the following section. To minimize fractional quantization noise, 20-GHz 16/17 pre-scalar is proposed. In section II, the suggested structures of VCO and pre-scalar are illustrated. In section III, the other circuits such as CP (Charge Pump), and PFD (Phase Frequency Detector) are illustrated. The measurement results are shown in section IV and the conclusions are drawn in section V.

II. Proposed Structure of the VCO and 16/17 Pre-scalar

As mentioned before, the requirement of the phase noise for the 60 GHz systems is lower than -90 dBc/Hz at 1 MHz offset frequency. The direct generation of the 60 GHz signal by CMOS VCO [2] showed a poor phase noise result mainly due to the passive losses from capacitors and varactors at 60 GHz frequency. The 60 GHz signal generated by push-push VCO [4] had harmonic and low output power problems. The injection locking oscillator [5] used two bulky additional LC tank oscillators that are susceptible to the process variation. It also took double the silicon die size comparing to other researches.

In order to resolve the phase noise issue, a 20 GHz only sliding IF architecture is proposed and illustrated in Fig. 1. Up/Down mixers are composed of 20 GHz mixers and 20 GHz sub-harmonic mixers. The 20 GHz sub-harmonic mixers translates 20 GHz input signal into 60 GHz output signal and vice versa. Therefore the VCO with the 20 GHz oscillation 20 GHz is the only local signal that is required for the 60 GHz system. By using one third of the system frequency, the design

issue to make low phase noise PLL is drastically mitigated.

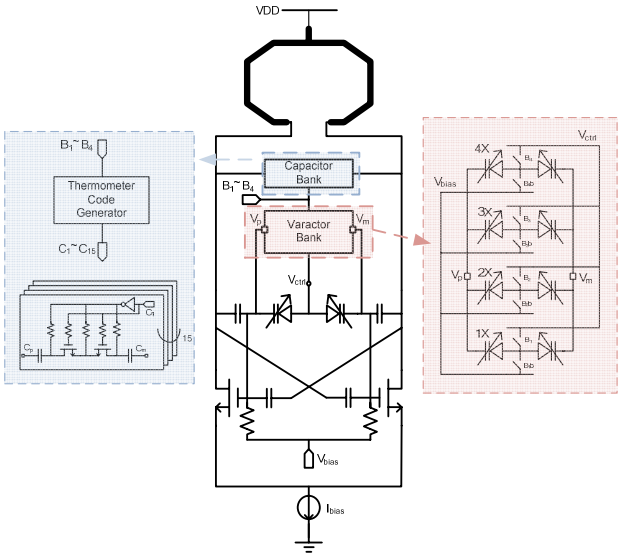

Fig. 2 Proposed VCO structure with Kv

Fig. 2 shows the proposed VCO structure. It is well known that the VCO with complementary gm cell has better phase noise performance than the N-MOS only structure. However, in the millimeter wave circuit, the parasitic capacitance introduced by P-MOS gm cell degrades phase noise performance further. Therefore N-MOS only cross coupled gm cell is applied in this paper.

The HFSS 3-D simulated differential inductor is adopted because required inductance value for LC oscillation is too small comparing to the inductance value in the PDK (Process Design Kit). To cover the whole frequency range of the 60 GHz system, the required VCO must have a feature of wide tuning range (large value of Kv). The noise generated by charge pump is multiplied by Kv and then translated into the phase noise of PLL. Moreover result of the trade-off relationship between loop bandwidth and VCO phase noise makes the in-band noise to be reckoned with. Thus 4-bit digitally controlled VCO is adopted to reduce the value of Kv and cover the whole frequency band at the same time. The 4-bit control signal goes through thermometer code generator and then controls fifteen capacitor switch arrays respectively. In this way, sixteen different resonance frequencies are generated by the switchable LC resonator and the effective value of Kv becomes 1/16 of the required value. As a result, in-band phase noise is reduced by 12 dB. Also to make every resonance condition of Kv constant, the 4-bit switchable varactor arrays are applied additionally. To lock the PLL, firstly the AFC block (in Fig. 1) selects the appropriate frequency code digitally and then the main PLL loop produces the right control voltage to VCO.

As mentioned before, PLLs for 60-GHz system were mainly integer type. The channel bonding introduced by ECMA standard, makes a fractional PLL synthesizer imperative in the future 60 GHz system. The bottleneck of designing the mm-waver fractional PLL is implementing high speed pre-scalar that is operated at 20 GHz. The designing is difficult due to a delay time of the modulus control (MC) is comparable

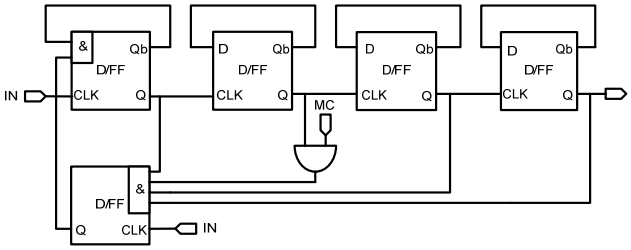

Fig. 3 Proposed block diagram of the 16/17 pre-scalar

to half of the operating period. One solution is using low speed pre-scalar by placing several stages of the static frequency dividers after VCO. However, the fractional quantization noise increases proportionally to the number of divider stages after the VCO because the controllable frequency step for the fractional generation is increased accordingly. Therefore, the best way for the low phase noise is to design speed of the pre-scalar as high as possible. While a 20 GHz pre-scalar was previously designed using SiGe process [6], the proposed 16/17 pre-scalar shows even faster speed in spite of using CMOS technology (See Fig. 3). The pre-scalar consists of CML D F/Fs and AND Gate imbedded CML D F/Fs. Implemented by the simple series and parallel transistor connection along with D F/F transistors, the imbedded D F/F improves the total delay property of the pre-scalar. Comparing to the previous work [6], the delay time of the MC signal is reduced considerably because the MC signal is pre-processed before the input of the second D F/F. The simulated result showed that the newly suggested structure has 20 % improved speed characteristics under same bias condition.

Along with the pre-scalar and reloadable/programmable counter [7], direct 20-GHz 8-bit programmable divider works well under the simulation and measurement. A MASH 1-1-1 type delta sigma modulator and a 50-MHz TCXO are used to generate stable output.

III. Remained Circuit Design

A CPPLL (Charge Pump PLL) is composed of PFD, CP, and LF (Loop filter). The reason for popularity of the CPPLL is because it provides the theoretical zero static phase offset, and arguably one of the simplest and most effective design. A PFD compares a TCXO signal and a divided VCO signal and produces two digital signals (Up and Down), with the width of these two signals being determined by their frequency and phase differences. The main building block of the PFD is D F/F which is designed by TSPC for low power and high speed. The designed PFD is depicted in Fig. 4. A Dead zone problem is solve be placing delay block after the NOR gate. When the clock signal is not applied, the output of the TSPC D F/F is un-known, which increases PLL locking time. To settle this problem, the latches (cross coupled inverters with different size) after the TSPC D F/F are adopted in this paper. To control

differential CP, the designed S-to-D block generates differential control signals and their symmetric wave forms are reinforced by the cross coupled inverters.

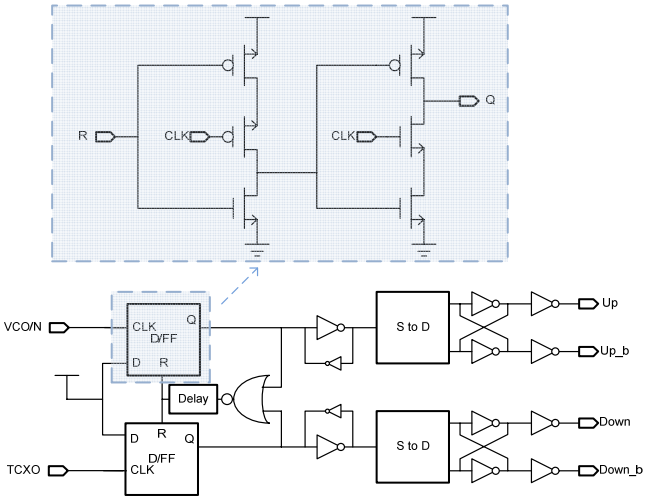

Fig. 4 Phase frequency detector with differential control output

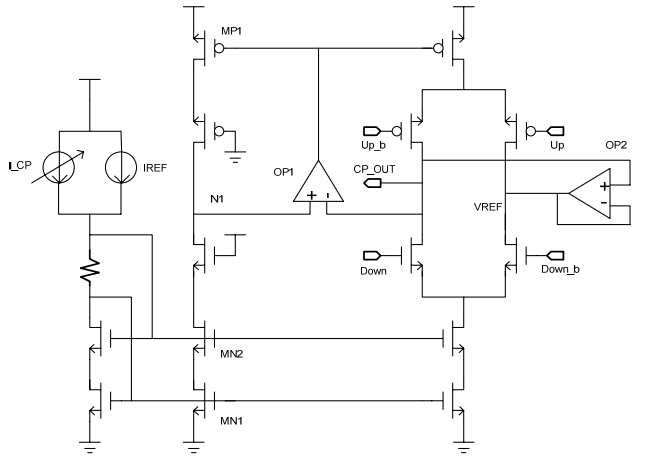

Fig. 5 Proposed charge pump circuit

The CP circuit is ideally parallel connection of current source and current sink which are implemented by PMOS and NMOS. However, the output resistance of the sub-micron transistor is not large enough to be modeled as a current source and sink. Therefore, a current mismatch occurs due to the difference between the drain-source voltages of the PMOS and NMOS when dumping the charge to the LF. A cascode structure boosts output resistance by the gain of the common source amplifier. However the cascode structure reduces voltage headroom and legroom of the CP output so the structure is not popular under the sub-micron technology. Another dominant problem in designing the low noise CP is charge sharing. When the CP switches are open, the drain voltage of PMOS is pre-charged to VDD and drain voltage of NMOS is discharged to GND due to the parasitic capacitance of the transistor. When the switches are closed, the output capacitor charges are shared with pre-charged or discharged parasitic capacitor which causes voltage ripple at every switching cycle.

Fig. 5 illustrates the designed CP circuit. The current sink is implemented with the cascode structure (MN1 and MN2).

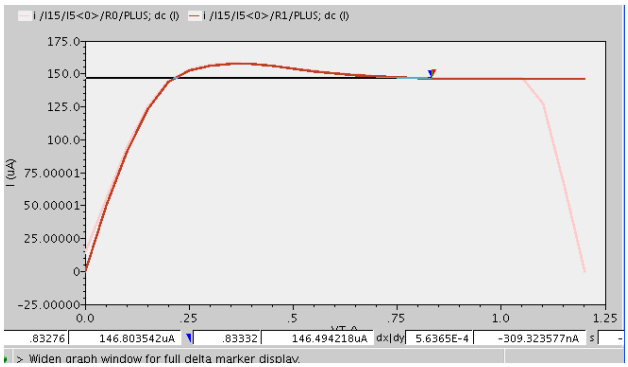

Fig. 6 Simulated DC characteristics of the proposed charge pump

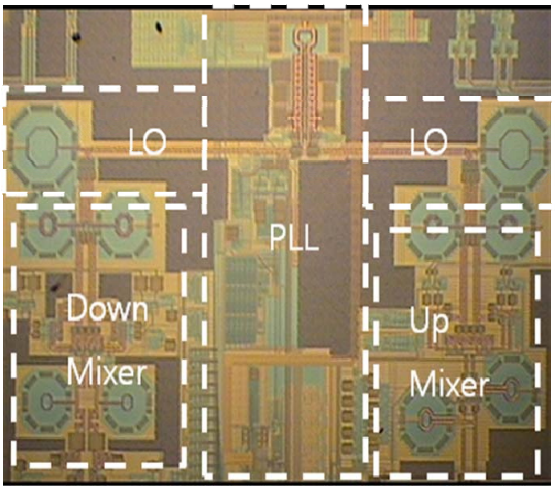

Fig. 7 Fabricated chip photo

The voltage legroom is secured by designing additional current source I_CP which is CP_OUT (output voltage) dependent (inversely proportional) current source. As the CP_OUT approaches to GND, more current is supplied to the CP then conduction current limitation caused by reduced legroom is compensated. The OP1 adjust gate voltage of MP1 with respect to the current of MN1. Also OP1 makes the node N1 the same with the CP_OUT, therefore the reference current is exactly mirrored to the core of the CP regardless of CP_OUT. In this way, current mismatch problem is minimized.

Differential architecture as shown in Fig. 5 guarantees constant current conduction to the CP core regardless of control signal. Constant current conduction mitigates charge sharing problems considerably, but the voltage difference between CP_OUT and VREF still generates charge sharing. The inserted OP2 is designed to eliminate above mentioned problem by making the two nodes equal. The simulation results show that the current mismatch is bounded within 300 nA with 0.2 ~ 1.1 V output operating range.

IV. Measurement Results

The Fig. 7 is the die photograph of the fabricated design using TSMC 90 nm CMOS process. The reference frequency of the TCXO used in this paper is 50 MHz. The circuit draws the maximum 30 mW for PLL from a 1.2 V supply. The measured PLL frequencies, 18.2 ~ 23.2 GHz, which are translated into 54.6 ~ 69.4 GHz covers all 60-GHz band with enough margin.

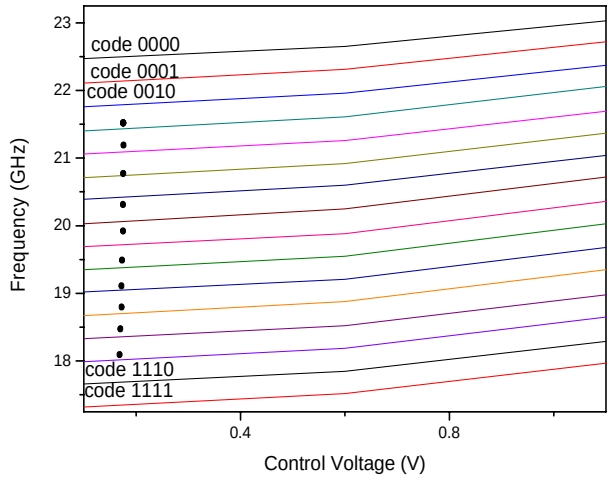

Fig. 8 Measured frequency characteristics of the PLL

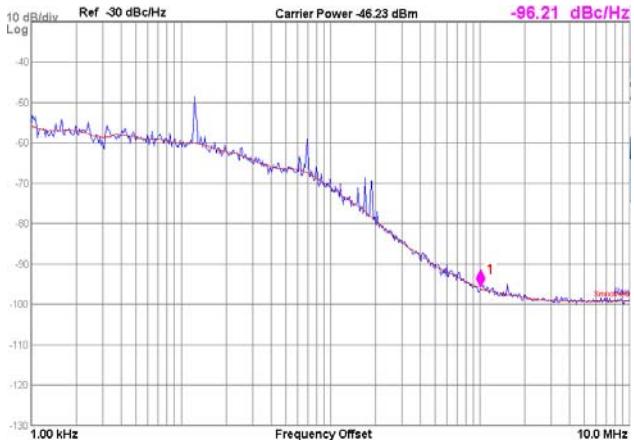

Fig. 9 Measured phase noise @ 20 GHz

The frequency range is measured by manipulating 8-bit integer programmable divider and 24-bit fractional SDM. Therefore the operation of the proposed pre-scalar is confirmed as far as 23.2 GHz. The measured tuning range is 25%. By using switchable fifteen capacitor arrays and four varactor arrays, the constant Kv is measured and well matched with simulation result (in Fig. 8). Due to the constant Kv, loop characteristics of all the resonance frequency is almost equal. The operational range of the CP is from 0.15 V to 1.09 V which is quiet well matched with simulation result. As a representative case, the phase noise of 20 GHz is selected and plotted in Fig. 9. A -58 dBc/Hz in-band noise and a -96.21 dBc/Hz noise at 1-MHz are measured. The measurement results shows that the proposed fraction PLL ensure 16 QAM data communication in 60 GHz frequency.

V. Conclusion

A mm-wave fractional PLL frequency synthesizer was implemented in 90 nm CMOS process. The proposed VCO showed wide tuning range and constant Kv characteristics due to the combination of the capacitor and varactor arrays. The 20-GHz pre-scalar worked well as high as 23 GHz. The measured frequency and voltage tuning characteristics were well matched with simulation. The proposed circuit met the phase noise requirement of the 60 GHz system. Thus, the presented design can be a good PLL candidate for 60 GHz high speed wireless communication.

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