Current Mode Logic Circuits for 10-bit 5GHz High Speed Digital to Analog Converter

Zhenguo Vincent Chia, Sheung Yan Simon Ng, and Minkyu Je

Abstract—This paper presents CMOS Current Mode Logic (CML) circuits for a high speed Digital to Analog Converter (DAC) using standard CMOS 65nm process. The CML circuits have the propagation delay advantage over its conventional CMOS counterparts due to smaller output voltage swing and tunable bias current. The CML circuits proposed in this paper can achieve a maximum propagation delay of only 9.3ps, which can satisfy the stringent requirement for the 5 GHz high speed DAC application. Another advantage for CML circuits is its dynamic symmetry characteristic resulting in a reduction of an additional inverter. Simulation results show that the proposed CML circuits can operate from 1.08V to 1.3V with temperature ranging from -40 to +120°C.

Keywords— Conventional, Current Mode Logic, DAC, Decoder.

I. INTRODUCTION

FOR many high resolutions high-speed DAC, the need for fast operating digital logic circuits is essential. With high speed digital circuits being used in many applications, such as digital TV and high-definition TV; this has increased the importance of designing digital logic circuits in subthreshold regime due to its reduced current and output voltage swing. In subthreshold MOSFET operation, current density is very low and the ratio of the transconductance to bias current of the device is maximum [1], [2].

This paper will discuss on the advantages of implementing CML circuits in high speed DAC. CML circuits have smaller dynamic power due to the reduced output voltage swing in high frequency operation. With reduced output voltage swing and fast logic switching, this allows CML circuits to be the best logic style for high speed mixed-signal design applications [5], [6]. Constant current supply of CML circuits further improves the accuracy of mixed-mode systems.

Usually for a thermometer decoder circuit, conventional CMOS circuits are used but there is a limit to how fast the circuit can operate. Conventional CMOS circuit is widely used due to the convenience of available standard library cells, small area, low power, and high noise margin [3]. In ideal operation, the conventional CMOS circuits have zero power consumption. During state transition, high current pulse is evident flowing

from supply to ground. When fast-state switching occurs at sub-GHz/GHz frequency range, high current spike can cause latch up which may destroy devices [4], [5].

Section II explains the motivation for CML circuits. Section III shows the application of CML circuits in a high speed decoder. Simulation results are presented in Section IV followed by an interpretation in Section V. Section VI contains a summary of the conclusions drawn from the study.

II. MOTIVATION FOR CML CIRCUITS

CML circuits do not require a rail-to-rail output swing, which is different from conventional CMOS circuits. The differential topology of CML circuits makes them resistant to common mode noise.

The first motivation to use CML circuits is that the switching speed is independent of the supply voltage, which is different from CMOS circuits. Thus, there is an operating range to achieve lower power dissipation without affecting performance. The delay of CML circuits is directly proportional to the resistance and capacitance:

$$\tau_{CML} = \frac{V_{swing}}{I} \bullet C = RC \qquad (1)$$

C is the output capacitive load. CMOS circuit has a delay time constant expressed as [9]:

$$\tau_{CMOS} = RC = C \bullet \frac{2V}{k \bullet (V - V_t)^\alpha} \qquad (2)$$

V and V_t are the supply and threshold voltages. The constants k and α depend on the process and transistor sizes. From (1) and (2), CML circuits are able to maintain the same performance at 1.2V or 0.8V, as compared to CMOS circuits which are guaranteed to suffer from performance degradation.

The second motivation relates to the low power dissipation of CML circuits in high operating frequency regime. In sub-GHz/GHz frequency applications, CMOS circuits are not very efficient due to the high dynamic power dissipation drawn from the fCV^2 relationship. However, the static power dissipation of CML circuits is independent of the operating frequency (f) due to the relatively constant current source in each logic gate circuit [10].

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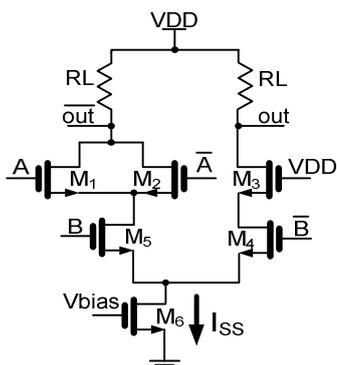
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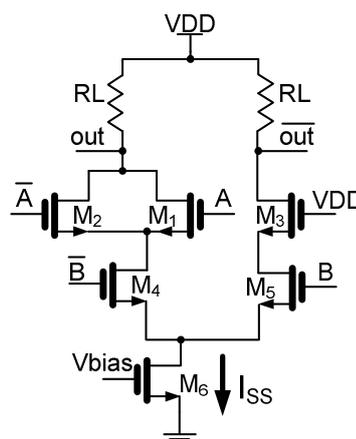
A. CML NAND/AND Logic

Fig. 1 CML NAND/AND logic schematic

Fig. 1 shows a simple two input NAND/AND gate with a passive load. This is one of the CML circuits that is used in the thermometer decoder. The purpose of M_3 is for level matching. M_6 supply the current bias for the whole logic circuit. The transistor channel length is sized larger to reduce the mismatch for current mirroring. Transistor, M_6 is bias at the saturation region to reduce the biasing current variation with different temperature from -40 to +120°C. This circuit is being designed for 400µA with supply voltage of 1.2V under typical condition. The switch transistors, M_1, M_2, M_4, and M_5 need to work at 5GHz, so the sizes need to be carefully design to reduce the parasitic capacitance at the input node. Transistors M_4 and M_5 are being size while keeping M_6 biased at the saturation region. The input voltages of 1.2 and 0.8V are supplied to M_4 and M_5. Simulating the DC operating point, the transistors are designed to be in saturation and subthreshold region. When the transistors operate correctly, a 5GHz frequency is supplied to the circuit to observe how the transistors behave.

As 0.8V is not low enough for the transistor to reach the cut-off region, one of the transistor pair M_4 or M_5 operates only at subthreshold region. The next pair of transistors is M_1 and M_2, while tuning the two transistors, it is important to note that while sizing of M_1 and M_2, special care is must be taken for M_4 and M_5. Therefore, there is always a tradeoff between a larger transistor and increasing rising time of the output signal. It is also important to note the current flowing in either of the two branches do not have high large leakage, as it cause a voltage drop across the load resistor where the output voltage does not reach VDD. The equation of voltage swing is

$$V_{swing} = R_L \bullet I_{SS} \qquad (1)$$

From (1), we can observe that resistor linearly affects the output voltage swing. The resister is kept constant. The resistor chosen must have the least resistance variance from -40 to 120°C. From datasheet given by the foundry, we chose a polysilicon OP resistor because it maintain restively constant throughout from -40 to +120°C.

B. CML NOR/OR Logic

Fig. 2 CML NOR/OR logic schematics

The 2-input CML NOR/OR logic circuit is similar to the one designed for the NAND/AND logic circuit. The differences between the two are the output nodes and the input signals.
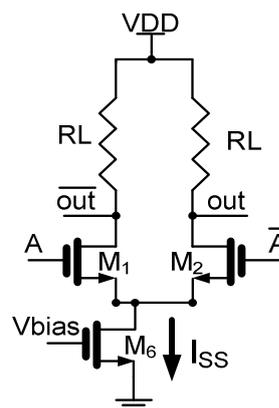
C. INV/BUFF Logic

Fig. 3 CML INV/BUFF logic schematic

The CML INV/BUFF circuit is the basic block for a simple digital logic. As mention before, DC operating point simulation for the INV/BUFF circuit is done using 0.8 and 1.2V. The first transistor to be size is M_6 where the transistor is in the saturation region; followed by the switching transistors M_1 and M_2 sized to operate in saturation and subthreshold region. After careful sizing M_1 and M_2 using static input, a dynamic input signal of 5GHz frequency is supplied to the circuit so that the output voltage swing is produce accordingly.

III. High Speed Thermometer-Coded Decoder

High speed thermometer-coded decoder is needed in DAC for high resolution decoding. Having to achieve accurate decoding is a challenge because at 5GHz, timing is a critical factor. In this 10bits DAC, full binary decoding is not preferred as it is very complex to be able to match all the transistors size for full 10bits. This affects the performance of the DAC in terms of monotonicity, Differential nonlinearity (DNL), and Integral nonlinearity (INL). Using fully thermometer coded is

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also not preferred as the area will be enormous and routing is almost impossible. With segmented decoding by splitting the Least Significant Bit (LSB) and Most Significant Bit (MSB) into binary and thermometer decoder respectively, both size and current matching is manageable. Since the current matching is easier for lower bits, thus binary decoding will be use for the 4LSB. Since binary is not practical to use in high bits, implementing thermometer decoding for the 6MSB is a viable way. For the thermometer decoder presented in this paper, CML circuits are implemented in the digital circuits. Binary-to-Thermometer decoders are used in both segmented and fully thermometer DACs [7]. A short example of 3 binary to 7 thermometer decoder as a conversion matrix is given by Fig. 4.

Fig. 4 3bits to 7 bits Thermometer Decoder

Fig. 5 shows the actual decoding circuit is achieved by using simple digital logic gates to drive the required current cells. To achieve the decoder function, two levels of logic circuits are required. B_4 to B_9 covers the MSB of the DAC that uses the thermometer decoder which is placed in row and column fashion. The latches placed between decoder and the matrix has two properties: (1) to reduce glitch effect, (2) to further improve the decoding speed [8].
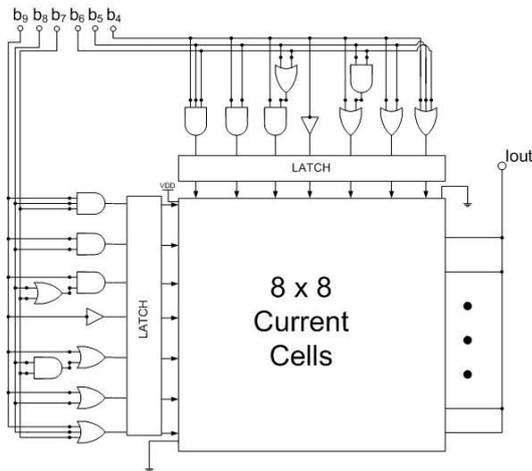

Fig. 5 High speed Decoder Circuit (CML)

The digital inputs are decoded in the row and column decoder. The number of flags, logic '1', in the rows corresponds to the column plus one. With some logic manipulation, the respective current cell will be turn 'ON'. The digital circuits shown above make use of the proposed CML

circuit technique to achieve high speed decoding circuit. We shall see how CML circuit performance as compared to the Conventional CMOS circuit, the results will be presented and interpreted in section IV and V respectively.

IV. SIMULATION RESULTS

The 6MSB thermometer decoder is implemented using Conventional CMOS and CML circuits. The simulation results are as follows.
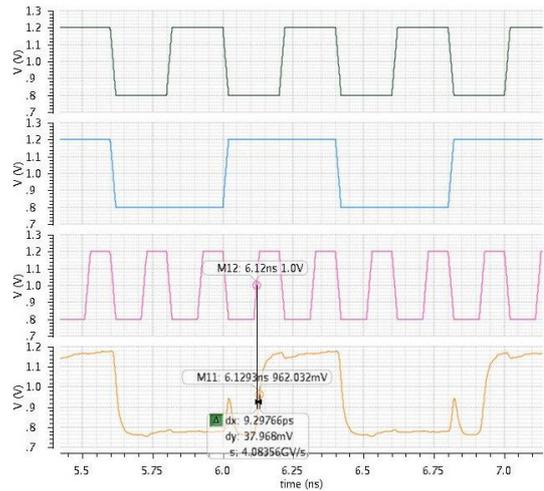

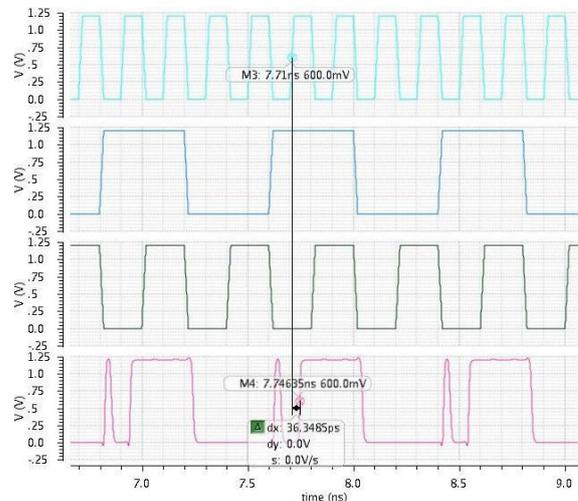Fig. 6 CML thermometer decoder under typical condition (1.2V @ 27°C with Delay = 9.3ps)

Fig. 7 CMOS thermometer decoder under typical condition (1.2V @ 27°C with Delay = 36.3ps)

From the thermometer decoder simulation results shown in Fig. 6 and Fig. 7, we observed that the result from the proposed CML circuits, delay time is shorter as compared to the conventional CMOS circuits. Not only does the delay improves, we also observed that the glitch in Fig. 6 is reduced compared to the result shown in Fig. 7. One of the reason is that the crossing of the digital input is at the midpoint during logic transiston. When two logic signals crosses at the same time, there will be a switching noise due to the pMOS and nMOS

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being turned on at the same time. This is not preferred as switching noise carries high current which can damage the transistors if care is not taken when sizing the transistors.

TABLE I
THERMOMETER DECODER PROPAGATION DELAY COMPARISON

Decoder	Time (picosec)	Percentage improvement
Conventional CMOS Logic	36.3	-
MCML Logic	9.3	79%

TABLE II
DESIGN SPECIFICATION

Criteria	Time (picosec)
Supply	1.2V
Speed	5GHz
Delay	<50

V. INTERPRETATION

The test conditions are presented in Table II, input voltage levels of 0.8V to 1.2V with supply of 1.2V at 27°C. In order to compare the two techniques (CML and CMOS circuits), a digital ramp signal is introduced to cycle through full eight binary logic levels (000 – 111). Having two 3 to 8 thermometer decoders, all 6MSB bits will be tested and the measurement is taken at the decoder output. The results are presented in Table I in Section IV. Comparing with the design specification shown in Table II, the delay time for CML circuit architecture is well within the criteria. Whereas for the conventional CMOS circuits, we observed that the delay is substantial. If an additional buffer is used, the delay time is not possible to meet the requirement. This can cause a missing code not decoded and degrade the overall performance of the DAC. In Table I, we observed that there is a significant improvement of about 79% for propagation delay over the conventional CMOS circuit. A 9.3ps of delay time enhance the logic accuracy when the data is being transferred from one stage to another. Having large propagation will eventually add delays to the following stage, for example, latch in Fig. 5, will fail to register the correct logic from the decoder if an inverter gate is added. It is seen that CML circuits can easily integrate with analog circuits.

VI. CONCLUSION

One possible implementation of CML circuits in thermometer coded is presented in this paper. The CML circuits' simulation results show a significant 79% of improvement in propagation delay. CML circuits' dynamic symmetry architecture can further reduce the delay time, this is possible due to the reduction of an additional inverter gate that conventional CMOS circuits need. Though CML circuits require static power, it improves the overall performance of the decoder by having less switching noise in which conventional CMOS circuits have. The reduction in switching noise can also reduce interference between analog circuits during integration as seen in Fig. 5.

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