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A Comparative Study of Electrical Transport Phenomena in Ultrathin vs. Nanoscale SOI MOSFETs Devices

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***Abstract*—**Ultrathin (UTD) and Nanoscale (NSD) SOI-MOSFET devices, sharing a similar W/L but with a channel thickness of 46nm and 1.6nm respectively, were fabricated using a selective "gate recessed" process on the same silicon wafer. The electrical transport characterization at room temperature has shown a large difference between the two kinds of devices and has been interpreted in terms of a huge unexpected series resistance. Electrical characteristics of the Nanoscale device, taken in the linear region, can be analytically derived from the ultrathin device ones. A comparison of the structure and composition of the layers, using advanced techniques such as Focused Ion Beam (FIB) and High Resolution TEM (HRTEM) coupled with Energy Dispersive X-ray Spectroscopy (EDS), contributes an explanation as to the difference of transport between the devices.

***Keywords*—**Nanoscale Devices, SOI MOSFET, Analytical Model, Electron Transport.

I. Introduction

NANOSCALE Silicon-On-Insulator (SOI) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) based devices are the building blocks of the up-to-date systems allowing ultra-fast data processing. This is in accordance with efforts to develop new generation of ultra-fast computers based on combined electronic and signal processing on one hand [1], and advanced generations of Nanoscale devices for communication systems [2], [3] on the other hand. In this article, a comparative study of the electrical characteristics of two kind of SOI MOSFET's is reported in order to explain the anomalous transport behavior of the thinner one having a channel thickness as low as 1.6 nm and obtained by a selective gate recessed process [4].

II. Experimental

A. SIMOX Preferred Wafer Processing Technology

Several techniques were developed in the past to create Silicon-On-Insulator (SOI) devices [5]-[8] since their implementation was found promising [9]-[11] for ULSI [12], low power [13], military and space [14], and cost reducing [15] applications. Nowadays, SOI wafers are mainly fabricated using the UNIBOND ® line of SOI wafers and the Smart Cut ® process technologies, patented by SOITEC Company, allowing excellent thickness uniformity [16]. However, for this research purpose, the former SOITEC technology called Separation-by-IMplanted-Oxygen (SIMOX) was preferred because of the clear advantage of presenting an initial gradient of the SOI thickness across the same wafer. This desirable gradient is conserved during the processing of the Nanoscale devices (NSD). Consequently, it is possible to study the thickness influence on the NSD electrical characteristics.

B. Buried Oxide Properties

In these SIMOX wafers, the Buried OXide (BOX) is performed by deep implantation of oxygen ions into silicon (p-type with a resistivity of 14–22 Ω.cm), using high energy of 120 keV and dose of 0.39 10^{18} ions O^{+}/cm^{2}. The ion implantation is performed at a temperature of 600°C for almost two and half hours. Then, an annealing phase of the silicon layer is performed at 1320°C for almost six hours [17]. Of course, change in implant parameters like energy, dose, and temperature may impact the thickness and the interface [18], [19]. The full process resulted in a BOX layer of 70nm under the mono-crystalline silicon (SOI) layer of 53nm. This technology has the advantage of offering an initial silicon thickness gradient that can be preserved during the fabrication process of nanoscale devices.

C. Thickness Cross-Characterization and Validation

By using a visible light spectrophotometer (FT750) providing multilayer thin films measurements (with layers typical thickness ranges down to 10 nm), the thickness of the SOI layer over the 6" SIMOX wafer was mapped and found varying between 49.83 to 59.40nm [20]. Usage of complementary thin films measurement methods such as ellipsometry, and HRTEM reinforced the thickness results with very high precision. To face the process tooling constraints, 2" diameter wafers had to be cut from the initial 6" SIMOX wafer. The largest thickness gradient zone (located at the opposite edge to the wafer flat) has been selected to be cut. After completing the thinning process (described below) the thickness of the silicon channel was mapped and was found to be varying between 1.64 to 6.57nm.

D. Furnace Accurate Calibration

The most challenging step was the accurate controlled

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thinning process of the SOI layer using local oxidation until reaching a 1.5 – 6.5nm range of thickness (Figs. 1 a and b), while the source and the drain regions remained in their original thickness. To check the capability of accurate thinning, preliminary tests of thinning were performed in order to reach thicknesses lower than 10nm, when characterizing the furnace parameters such as furnace temperature, duration of the oxidation, and growth rate [21].

E. Device Processing using Recessed-Gate Channel

The local oxidation was performed by using a nitride mask layer of 38nm (nitride 1) grown on a thin oxide layer (PAD OX) of 15nm. The role of the pad oxide was to serve as an interface between the nitride and the silicon in order to prevent mechanical stresses. A first etching of the nitride and pad oxide layer at the extremities of the active region allowed their oxidation into a 700nm thick Field Oxide (FOX). A second etching, performed in the center of the nitride region, allowed an exposure of the channel region while the surrounding nitride capped the source and drain areas. Two steps of oxidation were then performed: First, a 75nm thick sacrificial oxide layer, called Channel Oxide (CHAN OX) was grown in order to decrease the channel thickness to about 10nm in a more significant way, and then was finally removed. The second phase of the oxidation (26 nm thick), called Gate Oxidation (GOX), was a more accurate step allowing to reach the final Nanoscale thickness of the channel, in the range of 1.6nm to 6.5nm, and serving as the Gate Oxide itself, when the thickness distribution uniformity and the Si-SiO_2 interface quality [22] are serving as important parameters [23], [24]. In order to get reference devices on the same wafer, i.e. having an initial silicon channel close to 46 nm, the nitride mask was not etched so the gate insulator layer remained 38 nm thick nitride layer deposited on the 15nm PAD OX layer.

F. Contact Electrodes' Fabrication

A polycrystalline silicon layer of 220nm was deposited over the gate oxide, then oxidized, and patterned to form the gate electrode. Before the source/drain/gate phosphorus implant, a thin layer nitride (nitride 2) of 30nm was deposited in order to prevent further oxidation of the thin silicon layer during the implant's thermal annealing. A Plasma Enhanced Chemical Vapor Deposition (PECVD) oxide (Silox 2) of 350nm thickness was deposited followed by the aluminum metallization step to define the contact areas.

G. Electrical Transport Measurements' Set-Up

The I-V Characteristics' measurements (room temperature, dark conditions) were performed using the Semiconductor Characterization System (SCS-4200) from Keithley Ltd. The Devices Under Test (DUT) were packaged on a 24-DIP ceramic chip carrier and mounted on a commercial triax test fixture (Keithley model 8600) allowing a connection of up to four devices at a time.

III. Results and Discussion

A. Structural Characterization

Both representative SOI MOSFET devices having a same ratio W/L of 80/8 (μm) were analyzed using FIB and HRTEM techniques. A FIB cross-section of the Ultrathin Device (UTD) (46nm channel thick) is presented in Fig. 1 showing the device structure (Fig. 1 a) and the morphology of the layers forming the gate region (Fig. 1 b). A HRTEM zoom-in of the recessed silicon channel for the Nanoscale Device (NSD) is presented in Fig. 2, confirming the 1.6nm thickness value.

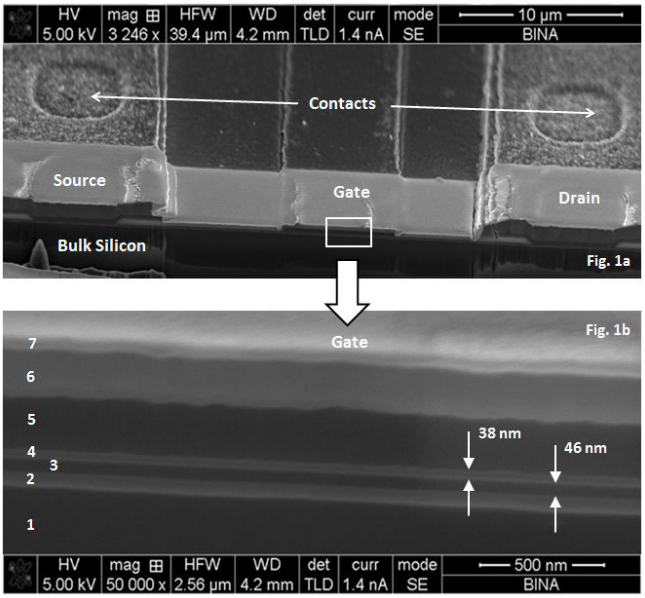

Fig. 1 a) FIB cross-section of the Ultrathin Device (UTD) (46nm channel thickness) showing the device structure including the source, gate and drain regions. b) Zoom in of the layers below the gate region: 1. Bulk silicon, 2. Buried oxide, 3. Silicon channel, 4. Nitride1/Gate Oxide, 5. Polysilicon, 6. Silox2/Nitride2, and 7. FIB metal deposition.

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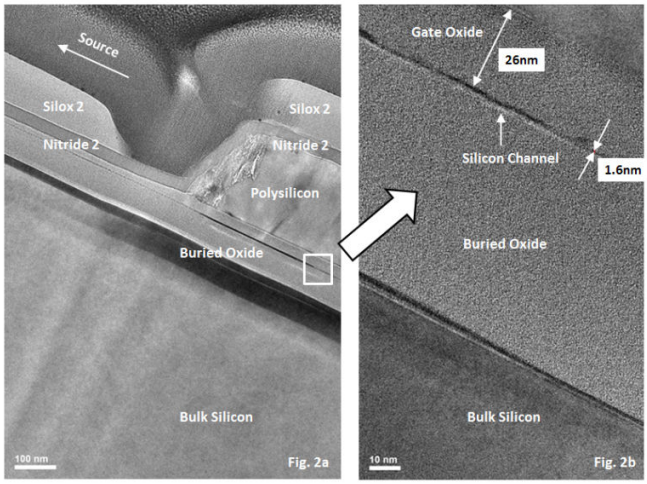

Fig. 2 a) HRTEM image of Nanoscale Device (NSD), showing a view of the gate's edge away from the source contact Since the edge of the source is located 10µm away from the Gate's edge, the source is not visible here. b) Zoom in below the Gate region reveals details of the recessed Silicon Channel and confirms the 1.6nm thickness value. Gate oxide thickness is 26 nm.

B. Electrical Characterization and Model

In Fig. 3 are presented the I_{DS}-V_{GS} measured characteristics (semi log scale) of the UTD when compared to the NSD's (solid lines). V_{DS} is kept constant to 0.4V which is close to the limit of the linear operation domain of the device [20].

Starting with UTD characteristic, it can be observed that for V_{GS} values more negative than -0.8 V, I_{DS} is slowly decreasing, and indicating a leakage phenomenon (negative resistance) similar to the Gate Induced Drain Leakage (GIDL) observed for both classic and SOI-MOSFET devices [25]. The same leakage phenomenon and amplitude are also measured for the NSD showing that the leakage is almost independent of the channel thickness as expected. Above -0.8 V the UTD characteristic is exponential (sub threshold region) with a relatively high swing value of 115 mV/dec ("ideal" value is ln(10)kt/q=60 mV/dec at room temperature). The threshold voltage V_T of the UTD is evaluated to -0.4V as extrapolated from the linear part of the I_{DS}-V_{GS} graph (not shown here). The effective mobility is derived from the dependence of the channel conductance g_d (as measured from I_{DS}-V_{DS} characteristics not presented here) on V_{GS}-V_T in the linear domain according to (1):

$$\mu_{eff} = \frac{g_d L}{W C_{gate} (V_{GS} - V_T)} \quad (1)$$

In UTD, the gate insulator is composed of a thin oxide layer (PAD OX) of 15nm thick and a nitride protective layer (again the recess oxidation process) of 38nm thick. Consequently, the gate capacitance C_{gate} is estimated to 121 nF/cm^2 and the Equivalent Oxide Thickness (EOT) is 28nm which is close to the NSD gate oxide thickness (25nm) as seen in Fig. 2 b). According to (1), μ_{eff} is decreasing from 1380 cm^2/Vs to 630 cm^2/Vs by increasing V_{GS} from 0 to 4V. The values are consistent with those obtained for similar SOI MOSFET devices [26]-[28].

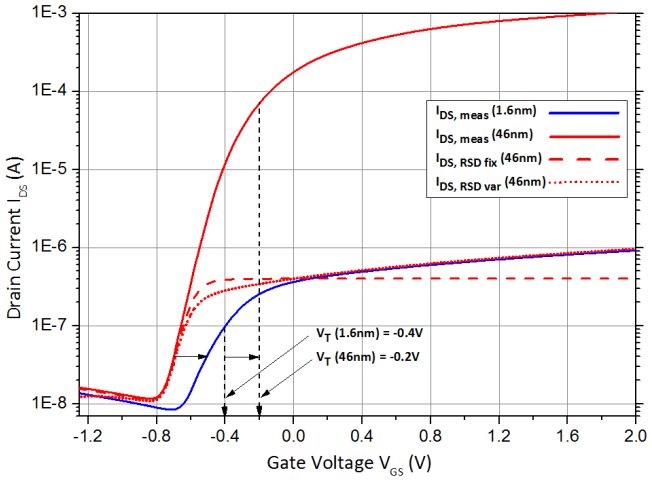

Fig. 3 I_{DS}-V_{GS} (semi-log) characteristics for Ultrathin Device (UTD) (46nm) and Nanoscale Device (NSD) (1.6nm) for V_{DS} = 0.4V.

As for the NSD characteristic, presented in Fig. 3 (solid line), above a V_{GS} value of -0.6V, I_{DS} is growing steeply in an exponential trend until -0.3V (subthreshold domain). The swing value is found surprisingly high (230 mV/dec) when compared to the previous UTD's value and also when compared to similar devices [29]. This result reveals an unexpected degradation of the subthreshold conduction correlated to the thinning process.

Another interesting fact noticed in Fig. 3, is that the subthreshold domain of the NSD is positively shifted by 0.2V relatively to the UTD device. Consequently, the NSD threshold voltage can be estimated to -0.2V. This result is consistent with the increasing of V_T in a comparable amount by thinning the channel below 10nm due to quantum mechanics considerations [30].

For positive V_{GS} values, the characteristic is bent and turned into a linear dependence on V_{GS}. Surprisingly, I_{DS} is measured to be three orders of magnitude lower than the UTD in the same region. Since the effective mobility (μ_{eff}) is limited to a minimum value of about 100-200 cm^2/Vs in Nanoscale SOI-MOSFET [31], [32] devices, the mobility variation as a function of the channel thickness cannot explain such a huge conductance attenuation. These characteristics are interpreted as resulting from the influence of a huge parasitic drain-source series resistance coupled with a gate leakage current that overwhelm the intrinsic channel resistance. The intercept value of I_{DS} at zero V_{GS} is about 0.4 µA for a V_{DS} value of 0.4 V. Assuming that V_{DS} value is only dropped by a series total resistance (R_{SD}=R_S+R_D), the R_{SD} value results in 1 MΩ. Varying V_{DS} had shown a linear dependence of I_{DS} with V_{DS} at zero V_{GS} confirming the assumption [20].

The influence of a series resistance R_{SD} on the drain current in the linear domain can be described by the following equation [33]:

$$For\ V_{GS} \geq V_T, I_{DS,lin} = \left(\frac{g_d}{1 + g_d R_{SD}} \right) V_{DS} \quad (2)$$

Using (2), a calculation can be done for the UTD's characteristic, disturbed by a fixed series resistance R_{SD} from the measured characteristic $I_{DS,\ meas,}$ and according to the following expression:

$$I_{DS,R_{SD}fix} = \frac{I_{DS,meas}}{1 + I_{DS,meas} \frac{R_{SD}}{V_{DS}}} \quad (3)$$

In Fig. 3, is presented the I_{DS}-V_{GS} characteristic (dashed line) of the UTD disturbed by a fixed series resistance R_{SD} of 1 MΩ according (3).

Indeed, (3) is equivalent to (2) in the linear domain (above -0.4 V) and is still valid in the subthreshold domain (below -0.4 V) since I_{DS}, meas become negligible relative to V_{DS} / R_{SD} i.e. 0.4μA. The calculated $I_{DS,RSD\ fix} - V_{GS}$ characteristic (dashed line) fits the NSD characteristic within the same order of magnitude but with a shift of -0.2V attributed to the difference of threshold voltage between the devices as mentioned above. However, for positive V_{GS}, the disturbed characteristic is a constant and then cannot fit the linear variation of I_{DS}.

In order to interpret this linear trend, a decrease of R_{SD} with V_{GS} can be considered, as observed in MOSFET's [34], according to:

$$R_{SD} = \frac{R_{SD0}}{1 + \theta V_{GS}} \quad (4)$$

In our NSD case, R_{SD} is 1 MΩ as mentioned above and θ was estimated to 0.70 [20].

Then, the calculated characteristic of the UTD disturbed by a variable series resistance R_{SD} can be re-written as:

$$I_{DS,R_{SD,var}} = \frac{I_{DS,meas}}{1 + I_{DS,meas} \frac{R_{SD0}}{(1 + \theta V_{GS}) V_{DS}}} \quad (5)$$

In Fig. 3, it is presented that the recalculated $I_{DS,\ RSD\ var}$ characteristic (dotted line), evaluated from (5), gave the best fit to the NSD characteristic. This helps to conclude that the characteristics of the NSD can be derived from the UTD by introducing a huge gate-controlled series resistance and by a positive shift of the threshold voltage.

IV. Physical Interpretation of the Electrical Model

Based on geometrical considerations, the difference of silicon channel thicknesses (factor 30) cannot in itself explain the difference in more than three orders of magnitude in the drain current. Secondly, phenomena that usually increase the spreading resistance, like the gradient of dopant concentration near the silicon channel extensions [34] and a gate mask mismatch, are not found relevant enough to explain the difference. But, as seen on Fig. 4, the gate-recessed process used to thin the channel has also squeezed the channel extensions located far from the gate region. Moreover, an Energy Dispersive X-ray Spectroscopy (EDS) was performed. It provides a local elemental analysis of the regions near the gate edge (EDS2) and further away (EDS3) in the source direction. It turns out that the later region (EDS3) still appears rich in oxygen (Si/O=2.5) and is comparable to the gate edge region (EDS2, Si/O=1.74). This over oxidation of the channel extensions can explain the apparition of a high series resistance.

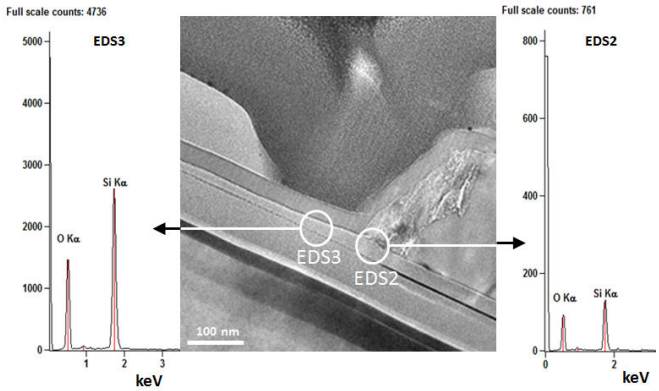

Fig. 4 EDS graphs representing the atomic concentration peaks of Silicon and Oxygen at two sites near the gate edge as shown on the corresponding HRTEM picture

V. Conclusions

Nanoscale SOI MOSFET devices were fabricated using a selective recess gate thinning process. I-V characteristics are measured and compared for the same W/L ratio to Ultrathin SOI MOSFET devices (non recess gate thinned). An abnormality of electrical transport (attenuation by three orders of magnitude of the drain current) is observed in the linear region for the Nanoscale device having a channel thickness as low as 1.6nm relative to the ultrathin device (46 nm channel thick). This result is interpreted and modeled analytically by introducing a huge gate controlled drain-source series resistance in the characteristics of the ultrathin device. This resistance seems to be due to an over oxidation of the channel extensions during the thinning process. The added value of this study is to provide an interpretative approach for modern Nanoscale devices, presenting disturbed electrical characteristics (high series resistance, mobility reduction, leakage current…), and which could be useful for prediction of transport phenomena at the Nanoscale.

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