Abstract-A 1V, 1GHz low noise amplifier (LNA) has been designed and simulated using Spectre simulator in a standard TSMC 0.18um CMOS technology. With low power and noise optimization techniques, the amplifier provides a gain of 24 dB, a noise figure of only 1.2 dB, power dissipation of 14 mW from a 1 V power supply.

I. INTRODUCTION

CMOS transistors have been consistently scaled to smaller feature sizes and continue to reduced towards sub-0.1um lengths. However, as the channel length decreases, so does the gate oxide thickness, dictating a decrease in the supply voltage. Commonly a low noise amplifier (LNA) is a key component in RF front-end receiver which poses a challenge in terms of meeting high gain, low noise figure and linearity requirement at low power supply(such as 1V). The primary role of the LNA is to lower the overall noise figure of the entire RF front-end, noise optimization is considered as one of the most critical steps in the LNA design procedure. 

The noise figure (NF) of LNA should not exceed a 3 dB, where the given system degrades the signal-to-noise ratio, which implies that higher gain and lower noise of LNA will lower the total noise of the system. Noise figure represents how much the given system degrades the signal-to-noise ratio, which is defined as:

\[ NF = 10 \log \frac{\text{Total Output Noise Power}}{\text{Output Noise Power Sourced to Impedance}} \]  

(2)

CMOS LNA design provides high level of integration at low cost but it is a big challenge to achieve low noise performance because of the noisy nature of MOS device. The dominant noise source in MOS devices is channel noise \[ g_{m} \] which results in:

\[ \frac{\gamma}{4kT}\delta_{d0} \]

(3)

Where \( g_{d0} \) is the zero-bias drain conductance of the device. \( \gamma \) is a bias dependent factor which, for long channel device satisfies \[ \frac{2}{3} \leq \gamma \leq 1 \], but for short channel devices can be as large as two or three, depending on bias condition. Another source of noise in MOS devices is the noise generated by the distributed gate resistance. This noise can be modeled by a series resistance in the gate circuit and an accompanying with noise generator, which results in:

\[ \frac{v_{g}^{2}}{8} = 4kTg_{f} \Delta f \]

(4)

where \( g_{f} \) is the coefficient of gate noise, normally equal to 4/3 for long channel devices and \( r_{g} \) is the gate resistance. The gate resistance can be minimized through interdigitation without the need of increased power dissipation, thus it is rendered insignificant [2]. If the sizes of the MOS transistors are carefully chosen, the optimum \( \omega_{0} \) which is simply a ratio of \( g_{m} / C_{g} \) can be obtained. Therefore, the minimum noise figure can be achieved according to [3]:

\[ F_{\text{min}} = 1 + \frac{n}{W} \sqrt{\frac{g_{m}}{C_{g}}} \left( 1 - |\delta|^2 \right) \]

(5)

If \( \delta \) were zero, the minimum noise figure would be 0dB[4].

II. NOISE FIGURE AND OPTIMIZATION

A. Noise Figure

An LNA determines the performance of the communication systems. It needs higher linearity and sufficient gain to overcome the next stage noise but not to overload. A system noise factor is defined as:

\[ F_{\text{total}} = F_{1} + \frac{F_{2} - 1}{G_{1}} + \frac{F_{3} - 1}{G_{1}G_{2}} + \ldots \]

(1)
B. Noise Optimization Techniques

A. Classical Noise Matching

In this technique, the LNA is designed for minimum NF by adding a matching circuit between the source and input of the amplifier [4]. By using this technique in Fig.1, at the input port in order to provide a 50 ohms impedance matching. There are several disadvantages in using this technique: The extra resistor contributes its own thermal noise to the output, which equals the noise contribution of the source resistance. This means that there would be an immediate 3dB increase in the noise figure. Furthermore, the input signal is attenuated by the resistor termination before reaching the active device, which causes a reduction in gain. Thus, one cannot obtain both input matching and minimum NF simultaneously. The large noise penalty due to the use of resistive termination is the main limitation of the classical noise matching.

B. Simultaneous Noise and Input matching

To achieve lower noise and higher gain, the cascode topology with the inductor degeneration topology is employed and shown in Figur 2.

Neglecting the gate drain capacitances, the input impedance of the LNA shown in Figure 1 is:

\[ Z_{in} = g_mL_s + \frac{1}{C_{gs}S} + s(L_s + L_g) + R_g \]

(6)

where \( g_m \) and \( C_{gs} \) are the transconductance and the gate-to-source capacitance of the input device \( M_1 \) respectively. \( L_g \) and \( L_s \) are the gate and source inductors and \( R_g \) is the effective gate resistance of \( M_1 \) given by \( R_g = R_0/\left(3n^2L\right) \) where \( R_0 \) is the sheet resistance of the gate polysilicon, \( W \) and \( L \) are the gate width and length of the transistor \( M_1 \) respectively and \( n \) is the number of fingers [2].

At the resonant operating frequency (\( \omega_0 \)), the input matching requires that:

\[ Z_{in} = R_s = \omega_0L_s \]

(7)

III. PROPOSED DESIGN APPROACH

For LNA design, inductive source degeneration is used to achieve good input matching without adding thermal noise introduced by real resistor. The cascode topology shown in Figure 2 is a popular configuration for LNA design, but it is not suitable for low voltage supply applications.

The proposed topology is shown in Figure 3, which works for low power supply applications such as 1V. Inductive source degeneration is also used to achieve good input matching and reduce noise figure. The first stage is inductively degenerated common-source amplifier formed by transistor \( M_0 \). Followed by a common-gate configured transistor \( M_1 \). The value of LC tank of \( M_0 \) is carefully chosen to achieve a resonance frequency of 1GHz and is required to have a much higher impedance than that of the input impedance looked at the source of
M₁. It provides a DC bias current path and a high impedance branch to force the RF signal to flow into the source of M₁ through a big DC coupling capacitance Cₛ.

The input impedance of the LC tank (Lₙ, Cₙ) is

\[ Z_d = R_d + \frac{\omega^2 L_d}{R_d} = \frac{\omega^2 L_d}{R_d} = R_d Q_d^2 \]  

Then,

\[ g_m = \frac{1}{R_d Q_d^2} \]  

where R_d and Q_d are the resistance and the quality factor associated with the inductor Lₙ.

The input impedance at the source of the common gate transistor M₁ is:

\[ R_f = \frac{1}{g_{m1} + g_{mb1} - 1} \approx \frac{1}{g_{m2}} \]  

where gₘ₁ is the bulk transconductance.

IV. Simulation Results

The complete circuit is shown in Figure 4. The LNA first

![Complete schematic of proposed common-source, common-gate LNA](image)

stage of the LNA M₀ transistor is inductively degenerated is a common-source amplifier followed by M₁ configured as common-gate device. M₀ sets the dc bias for M₀. M₂ is configured as the buffer stage for LNA output matching. C₁ between M₀ and M₁ is blocking DC and provides an ac path to let RF signal flow into the source of common-gate transistor M₁. In our case, it is designed to be 20 pF. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip. As shown in Figure 4 only the framed components are on-chip.

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process. Figure 5 shows a forward power gain (S₂₁) of 24 dB at 1 GHz. After noise optimization a low noise figure of 1.2 dB at 1 GHz is achieved and shown in Figure 6.

![Power gain of proposed LNA](image)

The S-parameters of the LNA are illustrated in Figure 7 and Figure 8 respectively. The S₁₁ shows a good input match of -21dB. The S₂₂ shows a good output match with the output buffer which achieves -15dB. The S₁₂ at 1GHz is -74.9 dB.
IIP3 simulation result of the LNA is shown in Figure 9. A two-tone signal which are chosen close to each other has been applied to the input port. The input-referred third-order intercept points (IIP3) is -29dBm. The layout of the LNA is shown in Figure 9. The chip area is 1mm x 1mm. This work is placed alongside with other recent reported LNA in Table 1. It shows that with the noise optimization techniques the proposed LNA achieves a much lower noise figure than other LNAs.

V. CONCLUSIONS

In this paper, a new CMOS low noise amplifier using common-source inductive source degeneration followed by common-gate configurations is proposed. The proposed topology is suitable for low power supply application and works good at 1 V voltage supply. Spectre simulation using TSMC 0.18µm CMOS technology shows a low noise figure of 1.2 dB, high power gain ($S_{21}$) of 24 dB and low power consumption of 14 mW from 1 V power supply.

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REFERENCES