High-performance Second-Generation Controlled Current Conveyor CCCII and High Frequency Applications

Néjib Hassen, Thouraya Ettaghzouti, Kamel Besbes

Abstract—In this paper, a modified CCCII is presented. We have used a current mirror with low supply voltage. This circuit is operated at low supply voltage of ±1 V. Tspice simulations for TSMC 0.18µm CMOS Technology have shown that the current and voltage bandwidth are respectively 3.34GHz and 4.37GHz, and parasitic resistance at port X has a value of 169.32Ω for a control current of 120µA.

In order to realize this circuit, we have implemented in this first step a universal current mode filter where the frequency can reach the 134.58MHz. In the second step, we have implemented two simulated inductors: one floating and the other grounded. These two inductors are operated in high frequency and variable depending on bias current I0. Finally, we have used the two last inductors respectively to implement two sinuosidal oscillators domains of frequencies respectively: [470MHz, 692MHz], and [358MHz, 572MHz] for bias currents I0 [80µA, 350µA].

Keywords—Current controlled current conveyor CCCII, floating inductor, grounded inductor, oscillator, universal filter.

I. INTRODUCTION

In recent years, the current conveyor has improved especially for high operating frequencies, low power and low supply voltage. The concept of circuit current controlled conveyor CCCII was introduced in 1995 [1]. These circuits based on modern electronics allow the design of many electronic functions as well as the voltage mode instead of the current mode. These circuits represent a logical evolution of second generation current conveyor. They become used in high frequency applications filtering [2]-[5] and oscillator [6]. The second generation current controlled conveyor has three port networks X, Y and Z, the relation between terminal voltage and current is given by the following matrix equation:

$$\begin{bmatrix} I_x \\ V_x \\ I_y \\ V_y \\ I_z \\ V_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & R_x & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & R_y & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_x \\ I_y \\ V_y \\ I_z \\ V_z \end{bmatrix}$$

(1)

The plus and minus signs in the third row specified the polarity of the current conveyor (CCCII+). Due to the architecture used for the design of CCCII, the circuit will introduce parasitic elements. The characteristic equation has become:

$$\begin{bmatrix} I_y \\ V_y \\ I_z \end{bmatrix} = \begin{bmatrix} Y_y & 0 & 0 \\ 0 & Z_x & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_x \\ I_z \end{bmatrix}$$

(2)

On the terminal Y and Z, two impedances Zy and Zz are specific to a parallel resistor with a capacitor. The impedance $Z_x$ on terminal X is a parasitic resistor $R_x$. Where $\alpha$ and $\beta$ denotes respectively current and voltage gains.

In this article, we have improved the current controlled conveyor. Subsequently, we will use it to implement a current mode universal filter. Second, we will use it to produce two inductors: floating and tied to ground. Based, on these last two experiences, we have made two oscillators functioning at high frequency.

II. NEW CCCII CONFIGURATION

The circuit current controlled conveyors CCCII classic introduced by [7]-[11] is shown in Fig.1.a. In intention to ameliorate bandwidth in current mode of this circuit, we present two current mirrors FVF (M8, M9, and M14) and (M12, M13, M16) which works in low voltage and characterized by low input impedance [12]-[15] (Fig.1.b). The two current mirrors can duplicate the current in the borne X on to the borne Z. The transistors M14 and M16 are used to adjust the linearity of the transfer characteristic of two mirrors of the output current and have currents in the paths equal X and Z ($I_x = I_L = I_{G1} - I_{G0}$).

The second property of CCCII is a voltage follower between terminal X and Y, the last pair is linked together by a mixed trans-linear loop (M1, M2, M3, M4).

$$V_{yy} = (V_{GS1})_p - (V_{GS4})_p = (V_{GS1})_N - (V_{GS2})_N$$

(3)

With:

$$V_{GS} = \frac{(I_d)_p}{\frac{1}{2} \mu C_{ox} \frac{W}{L}} + V_{THp}$$

and

$$V_{GS} = -\frac{(I_d)_N}{\frac{1}{2} \mu C_{ox} \frac{W}{L}} + V_{THn}$$

The current through transistors M1 and M3 is equal to $I_0$. In this case, the potential difference $V_{xy}$ is equal to:
By identifying the characteristic equations CCCII circuit, we have:

\[ R_x = \frac{I}{\sqrt{2I_L C_{ox}(\mu_p \frac{W}{L})_p + \sqrt{\mu_n \frac{W}{L}}}} \]

(7)

If \( \mu_p \frac{W}{L} \) \( \mu_n \frac{W}{L} \)

The expression of input resistance becomes:

\[ R_x = \frac{1}{\sqrt{8C_{ox} \mu_p \frac{W}{L} I_0}} \]

(8)

To achieve a current controlled conveyor with negative transfer (CCCII-), we just need to reverse the current in the terminal \( Z \). This inversion is carried out in two additional current mirrors (M1P, M2P) and (M1N, M2N) whose entries are crossed [16]-[19] (Fig. 2).

A. Simulation Results of CCCII

The results are optimized by the size of transistors summarized in Table I and II for a bias current \( I_0 \) of 120\( \mu \)A and a supply voltage of \( \pm 1 \)V. These different schemes are simulated using Tspice based BSIM3v3 transistor model for the TSMC 0.18\( \mu \)m CMOS process available from MOSIS [20].

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W/L</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>60 ( \mu )m /0.18 ( \mu )m</td>
</tr>
<tr>
<td>M3, M4</td>
<td>90 ( \mu )m /0.18 ( \mu )m</td>
</tr>
<tr>
<td>M5, M6</td>
<td>20 ( \mu )m /0.18 ( \mu )m</td>
</tr>
<tr>
<td>M7</td>
<td>22 ( \mu )m /0.18 ( \mu )m</td>
</tr>
<tr>
<td>M8, M9</td>
<td>28 ( \mu )m /0.18 ( \mu )m</td>
</tr>
<tr>
<td>M10, M11</td>
<td>2 ( \mu )m /0.18 ( \mu )m</td>
</tr>
<tr>
<td>M12, M13</td>
<td>17 ( \mu )m /0.18 ( \mu )m</td>
</tr>
</tbody>
</table>

Fig. 1 Circuit current controlled conveyor CCCII (a) Classic (b) Modified

\[ V_y \equiv V_y = \frac{I_x}{\sqrt{2I_L C_{ox}(\mu_p \frac{W}{L})_p + \sqrt{\mu_n \frac{W}{L}}}} \]

(6)

By determining relationships \( I_{x2} \) and \( I_{x4} \) according to \( I_0 \) and \( V_{xy} \) from (4) and (5) and applying the relationship \( I_x = I_{x2} - I_{x4} \) and after taking everything into account we find:

\[ V_{xy} = (V_{GS1})_N - (V_{GS2})_N = -\frac{I_0}{2 \mu_p C_{ox} \frac{W}{L} N} + \frac{(I_{x2})_N}{2 \mu_p C_{ox} \frac{W}{L} N} \]

(4)

\[ V_{xy} = (V_{GS3})_N - (V_{GS4})_N = -\frac{I_0}{2 \mu_p C_{ox} \frac{W}{L} P} + \frac{(I_{x4})_P}{2 \mu_p C_{ox} \frac{W}{L} P} \]

(5)

Fig. 2 Block circuit output current controlled conveyor transfer negative
TABLE II

DIMENSIONS OF TRANSISTORS OF AMENDED CCCII

<table>
<thead>
<tr>
<th>Transistors</th>
<th>W / L</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2</td>
<td>60 µm /0.18 µm</td>
</tr>
<tr>
<td>M3, M4</td>
<td>90 µm /0.18 µm</td>
</tr>
<tr>
<td>M5, M6</td>
<td>20 µm /0.18 µm</td>
</tr>
<tr>
<td>M7</td>
<td>22 µm /0.18 µm</td>
</tr>
<tr>
<td>M8, M9</td>
<td>10 µm /0.18 µm</td>
</tr>
<tr>
<td>M10, M11</td>
<td>2 µm /0.18 µm</td>
</tr>
<tr>
<td>M12, M13</td>
<td>8 µm /0.18 µm</td>
</tr>
<tr>
<td>M14</td>
<td>22 µm /0.18 µm</td>
</tr>
<tr>
<td>M15</td>
<td>0.55 µm /0.18 µm</td>
</tr>
<tr>
<td>M16</td>
<td>12 µm /0.18 µm</td>
</tr>
<tr>
<td>M17</td>
<td>1.52 µm /0.18 µm</td>
</tr>
</tbody>
</table>

B. Simulation Static

The Fig.3.a represents the characteristic transfer of output current $I_z$ according to $I_x$ in the range $\pm 0.7$ mA. The linearity error is shown in Fig.3.b. It does not exceed 0.8% in the range $\pm 0.35$ mA for the improved circuit. In contrast, the reference circuit, this error is much greater approximation of 5% over the same interval. The change in input resistance as a function of bias current $I_0$ is shown in Fig.4.

C. Simulation AC

Dynamic simulation is for a resisting load of 1kΩ. The frequency response of the current gain is shown in Fig.6.a. The bandwidth of the current gain at -3dB is 3.34GHz instead of 1.45GHz. Dynamic simulation mode voltage (Fig.6.b) gives a bandwidth of 4.37GHz and a static gain of 0.948. In Table 3, we have synthesized all the results of circuit simulation with the modified circuit of [8], [9], [11].
### TABLE III
SIMULATION RESULTS OF CIRCUIT CCCII

<table>
<thead>
<tr>
<th></th>
<th>Modified circuit</th>
<th>Classic circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18µm TSMC</td>
<td>0.18µm TSMC</td>
</tr>
<tr>
<td>Bias voltage (Vcc-Vss)</td>
<td>2V</td>
<td>2V</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>0.948</td>
<td>0.948</td>
</tr>
<tr>
<td>Current gain</td>
<td>1</td>
<td>0.97</td>
</tr>
<tr>
<td>Bandwidth current Fci</td>
<td>3.34GHz</td>
<td>1.45GHz</td>
</tr>
<tr>
<td>Bandwidth voltage Fcv</td>
<td>4.37GHz</td>
<td>5.38GHz</td>
</tr>
<tr>
<td>Error voltage (±0.4V) (%)</td>
<td>1.5</td>
<td>2.3</td>
</tr>
<tr>
<td>Error current (±0.35mA) (%)</td>
<td>0.8</td>
<td>5.16</td>
</tr>
<tr>
<td>Input resistor Rx</td>
<td>169.32Ω</td>
<td>196Ω</td>
</tr>
<tr>
<td>Input Impedance (Ri/Ci)</td>
<td>5.67KΩ//164fF</td>
<td>8.12KΩ//149fF</td>
</tr>
<tr>
<td>Output impedance (Ro/Co)</td>
<td>6.81KΩ//37.5fF</td>
<td>0.876KΩ//108.01fF</td>
</tr>
<tr>
<td>THD at 1 MHz @ 0.3mA</td>
<td>0.24%</td>
<td>0.86%</td>
</tr>
<tr>
<td>THD at 1 MHz @ 0.3V</td>
<td>0.41%</td>
<td>0.47%</td>
</tr>
</tbody>
</table>
III. APPLICATIONS

A. Universal Filter

Circuit current conveyors are widely used in filtering applications. In recent years, several studies have been made specifically to improve the universal filter [2]–[5], [21]–[31]. We will use three circuits current controlled multi-output (MOCCCII) (Fig. 7) to achieve a universal filter current-mode [7].

\[
\begin{align*}
I_{LP} &= \frac{R}{R_{C1} + p^2 + \frac{1}{R_{C1} C_1 C_2}} \left( -\frac{1}{R_{C2} C_2} \right) \\
I_{HP} &= \frac{R}{R_{C1} + p^2 + \frac{1}{R_{C1} C_1 C_2}} \left( \frac{1}{R_{C2} C_2} \right) \\
I_{BP} &= \frac{R}{R_{C1} + p^2 + \frac{1}{R_{C1} C_1 C_2}} \left( \frac{1}{R_{C2} C_2} \right) \\
I_{AP} &= \frac{R}{R_{C1} + p^2 + \frac{1}{R_{C1} C_1 C_2}} \left( \frac{1}{R_{C2} C_2} \right)
\end{align*}
\]

Fig. 7 Diagram of universal filter based on three MOCCCII

The transfer functions of the universal filter: Low-pass, High-pass, Band-pass, Notch and All-pass are given respectively by the following expressions

\[
\begin{align*}
I_{LP} &= \frac{R}{R_{C1} + p^2 + \frac{1}{R_{C1} C_1 C_2}} \left( -\frac{1}{R_{C2} C_2} \right) \\
I_{HP} &= \frac{R}{R_{C1} + p^2 + \frac{1}{R_{C1} C_1 C_2}} \left( \frac{1}{R_{C2} C_2} \right) \\
I_{BP} &= \frac{R}{R_{C1} + p^2 + \frac{1}{R_{C1} C_1 C_2}} \left( \frac{1}{R_{C2} C_2} \right) \\
I_{AP} &= \frac{R}{R_{C1} + p^2 + \frac{1}{R_{C1} C_1 C_2}} \left( \frac{1}{R_{C2} C_2} \right)
\end{align*}
\]

The proper frequency \(f_0\) and the gain \(G_0\) of the current mode universal filter are given by the following terms:

\[
f_0 = \frac{1}{2\pi R_{C1} R_{C2} C_1 C_2} \quad (14)
\]

\[
G_0 = \frac{R}{R_{C1}} \quad (15)
\]

To confirm the theoretical results obtained, we have performed simulations based on CMOS technology Tspice with TSMC 0.18µm and with a voltage bias of ±1V. The bias currents of CCCII three circuits are equal to 120µA. The values of passive components used are \(C_1=C_2=15\text{pF}\) and \(R=R_{X}\). Subsequently, we have obtained a center frequency of 67.45MHz (Fig. 8). In the contrast with the calculated theoretical value which is about 62.7MHz.

![Fig. 8 Result of simulation of the module universal filter](image)

![Fig. 9 Change in frequency as a function of bias current](image)

The variation of \(f_0\) based bias current \(I_0\) is shown in Fig. 9, with \(C_1=C_2=15\text{pF}\).

Table IV shows the comparison of our results with other work on the current-mode universal filter.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Information about the circuit</th>
<th>Numbers of active elements</th>
<th>Center frequency (MHz)</th>
<th>Quality factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2]</td>
<td>0.5µm CMOS Spice Vcc=Vss=6V</td>
<td>4-DOICCII</td>
<td>10MHz</td>
<td>0.707</td>
</tr>
<tr>
<td>[3]</td>
<td>0.35µm TSMC H-Spice Vcc=Vss=1.65V</td>
<td>3-MOCCCII</td>
<td>110KHz</td>
<td>1</td>
</tr>
<tr>
<td>[5]</td>
<td>0.18µm CMOS T-Spice Vcc=Vss=±1V</td>
<td>3-MOCCCII</td>
<td>134.58MHz</td>
<td>1</td>
</tr>
<tr>
<td>Our results</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
B. Implementing an inductance

This problem has drawn the attention of many researchers. They have decided to make inductors based on active elements such as current conveyors, resistors and capacity. In this section, we present the creation of types of inductors, floating and related to ground, based on CCCII circuit modified.

1. Floating inductor

Scheme of a floating active inductor using four CCCII+ [33]-[35] is shown in Fig.10.

![Diagram of Floating Inductor](image)

The circuits CCCII 1 and 2 are biased by an identical current $I_{01}$, so that the capacitance $C$ is covered by the same current. Similarly, the conveyor CCCII 3 and 4 are biased by $I_{02}$ to have equal currents in A and B. $R_{x1}$ is the parasitic resistance associated with the CCCII1 and 2 for the current $I_{01}$. Similarly, $R_{x2}$ is the parasitic resistance associated with the CCCII3 and 4 for the current $I_{02}$.

$$V_{AB} = 2R_{x1}I_1$$
$$V_i = \frac{1}{pC}I_1 = 2R_{x2}I_{in}$$
$$V_{AB} = p(2R_{x1})/(2R_{x2})CI_{in}$$
$$L = (2R_{x1})\times(2R_{x2})C$$

2. Inductor connected to ground

Subsequently, based on [33]-[37], we have introduced another inductor based two current conveyor, one with positive transfer and the other with negative transfer and capacity.

![Diagram of Inductor Connected to Ground](image)

The implementation of this inductance is illustrated in Fig.11. Taking into account the presence of parasitic resistors $R_{x1}$ and $R_{x2}$:

$$V_{in} = V_{x1} = -R_{x1}I_{s1}$$
$$V_{y2} = V_{x2} = -\frac{1}{jC}\omega I_{s2} = R_{x2} I_{in}$$

According to equation (21), we have:

$$I_{s1} = -jR_{x2}C\omega I_{in}$$

The confusion of two expressions (20) and (22) gives:

$$Z_{in} = \frac{V_{in}}{I_{in}} = jR_{s1}R_{x2}C\omega$$

It is equivalent to an inductance $L$ for:

$$L_{eq} = R_{s1}R_{x2}C$$

3. Simulation results

In both structures, we have minimized the number of circuits used. We have used only the conveyors current to single output and only one capacity. Both inductors have an operating frequency zone and $L$ values vary with bias current $I_0$. At each change in bias current $I_0$, we have found the area of operation frequency with an accuracy of ± 5 degrees of phase (table 5).
We have given the importance of oscillators in the field of signal processing; many researchers have proposed many structures to improve their frequency performance, low power and low voltage. The proposed oscillator circuit based on an operational amplifier is shown in Fig.12.

Based on the equivalent circuit, the network reaction has as input impedance:

\[ Z_{in} = Z_j/(Z_3 + Z_j) = \frac{Z_3 (Z_2 + Z_1)}{Z_1 + Z_2 + Z_3} \]  

(26)

The transfer function of the amplifier:

\[ H = \frac{V_o}{V_{in}} = \frac{A \cdot V_{in}}{Z_{in} + R_{in}} = \frac{A \cdot Z_{in}}{R_{in} + Z_{in}} \]  

(27)

With \( A \): The gain of the direct chain. \( A_0 = -\frac{R_2}{R_1} \).

\( R_c \): The output resistance characteristic of the amplifier.

The transfer function of the chain reaction is given by

\[ K = \frac{V_{in}}{V_o} = \frac{Z_1}{Z_1 + Z_2} \]

According to the Barkhausen condition \( H \times K = 1 \).

We have:

\[ A_0 Z_2 Z_3 = R_0 (Z_1 + Z_2 + Z_3) + Z_4 (Z_2 + Z_1) \]

With \( Z_i = j X_i, i = 1, 2, 3 \)

The oscillation condition becomes;

\[- A_0 X_1 X_2 = j R_0 (X_1 + X_3 + X_4) - X_2 (X_2 + X_4) \]

In our case \( A_0 < 0 \), by identifying:

\[ A_0 X_i = -X_3, X_1 \text{ and } X_2 \] have the same sign as in both similar components

\( X_1 + X_2 + X_3 = 0 \), the second condition requires \( X_2 \) component of a different nature.

Based on some work [38]-[40], we have transformed the oscillator circuit of Fig.12 based conveyor CCCII as shown in Fig.13. This figure shows two types of oscillators: the first based on an inductor connected to ground (Fig.13.a) and the second based on a floating inductance (Fig.13.b). We used the same reactors studied previously.

A basis of an inductor connected to ground, this circuit has an oscillation frequency and gain:

\[ f_o = \frac{1}{2 \pi \sqrt{(L_1 + L_2) C}} \]  

(28)
\[ A_0 = -\frac{L_2}{L_1} = -\frac{R_2}{R_1} \]  

(29)

A basis of a floating inductor, the circuit has an oscillation frequency and gain:

\[ f_0 = \frac{I}{2\pi \sqrt{C_1 C_2 \frac{1}{C_1} + \frac{1}{C_2} L}} \]  

(30)

\[ A_0 = -\frac{C_1}{C_2} = -\frac{R_2}{R_1} \]  

(31)

We performed simulations with a supply voltage of ± 1V. The choice of components is as follows: \( C = 100\, \text{nF} \) to the first circuit and \( C_1 = C_2 = 0.1\, \text{pF} \) for the second with the condition \( R_2 = 10\, R_1 \). By the current variation of \( I_0 = [80\, \mu\text{A}, 350\, \mu\text{A}] \), we obtained an oscillation frequency variable \([358\, \text{MHz}, 572\, \text{MHz}]\) and \([470\, \text{MHz}, 694\, \text{MHz}]\), respectively the first and second circuit (Fig.14)

For a bias current \( I_0 = 120\, \mu\text{A} \), the signal of the oscillator is shown in Fig.15

![Diagram](image_url)

Fig. 13 Implementation of two oscillator circuit based on CCCII
(a). a basis of an inductor connected to ground (b). a basis of a floating inductor

![Diagram](image_url)

Fig. 14 Frequency of the oscillator based on current \( I_0 \)
(a). A basis of an inductor connected to ground (b). A basis of a floating inductor

![Diagram](image_url)

Fig. 15 Output signal of the oscillator (a). A basis of an inductor connected to ground (b). A basis of a floating inductor
IV. CONCLUSION

In this paper we have made several improvements to the circuit current conveyor CCCII controlled using current mirrors with low supply voltage. This circuit operates at low supply voltage of ±1V and present to a bias current of 120µA, a bandwidth of 3.34GHz and 4.37GHz respectively in current mode and voltage mode for expenses and a 1kΩ parasitic resistance Rx of 169.32 Ω. Based on this circuit, we have implemented first a universal filter, current mode. The frequency can reach the 134.58MHz. In the second, we have implemented two inductors, one floating and the other tied to ground, operating in high frequency and variable depending on bias current I0. We have used the last two, respectively, to implemented two sinusoidal oscillators frequency one [358MHz, 572MHz], second [470MHz, 692MHz] for bias currents I0 [80µA, 350µA].

REFERENCES
Néjib HASSEN was born in 1961 in Moknine, Tunisia. He received the B.S. degree in EEA from the University of Aix-Marseille I, France in 1990, the M.S. degree in Electronics in 1991 and the Ph.D. degree in 1995 from the University Louis Pasteur of Strasbourg, France. From 1991 to 1996, he has worked as a researcher in CCD digital camera design. He implemented IRDS new technique radiuses CCD noise at CRN of GOA in Strasbourg. In 1995, he joined the Faculty of Sciences of Monastir as an Assistant Professor of physics and electronics. Since 1997, he has worked as researcher in mixed-signals neural networks. Actually he is focusing on the implementation low voltage - low power circuits.

Thouraya Ettaghzouti was born in Tozeur, Tunisia, in 1983. She received the B.S. degree from the Faculty of Sciences of Monastir in 2008, the M.S. degree from at the same University at the Microelectronic and Instrumentation Laboratory in 2010. Actually, she is preparing the Ph.D degree. She is interested to the implementation of low voltage low power integrated circuit design.

Kamel BESBES was born in Monastir, Tunisia, in 1960. He received the B.S. degree from the Faculty of Sciences of Monastir in 1985, the M.S. degree from the Ecole Centrale de Lyon, Lyon, France, in 1986, the Ph.D. degree from the Institut National des Sciences Appliquées de Lyon (INSA), Lyon, in 1989, and the Doctorat d'Etat degree from the Faculty of Sciences of Tunis, Tunisia, in 1995. In 1989, he joined the Faculty of Sciences of Monastir as an Assistant Professor of physics and electronics. He is now a Professor and the Dean of the Faculty and the Head of the Microelectronics and Instrumentation Laboratory. His research work and interest are focused on microelectronics, modeling, and instrumentation.