A Power Reduction Technique for Built-In-Self Testing Using Modified Linear Feedback Shift Register

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Abstract—A linear feedback shift register (LFSR) is proposed which targets to reduce the power consumption from within. It reduces the power consumption during testing of a Circuit Under Test (CUT) at two stages. At first stage, Control Logic (CL) makes the clocks of the switching units of the register inactive for a time period when output from them is going to be same as previous one and thus reducing unnecessary switching of the flip-flops. And at second stage, the LFSR reorders the test vectors by interchanging the bit with its next and closest neighbor bit. It keeps fault coverage capacity of the vectors unchanged but reduces the Total Hamming Distance (THD) so that there is reduction in power while shifting operation.

Keywords—Linear Feedback Shift Register, Total Hamming Distance, Fault Coverage, Control Logic

I. INTRODUCTION

Power Dissipation is a challenging problem in today’s System-on-Chips (SoC) Design and Test. In general, power dissipation of a system in test mode is more than that in normal mode. This is because a significant correlation exists between the consecutive test vectors applied during the circuit’s normal mode of operation, whereas this may not be necessarily true for applied test vectors in test mode of operation. Low correlation between test vectors increases switching activity and eventually leads to power dissipation in the circuit.

Built-In Self Test (BIST) is the most suitable approach for low power testing as it provides a larger scope for low power techniques to be used. BIST uses an LFSR as test pattern generator (TPG). The LFSR generates all possible test vectors increases switching activity and eventually leads to power dissipation in the circuit.

In BIST, LFSR is an important module. Several modified versions of LFSR have been proposed which consume relatively little power. Gated clock design of LFSR is found in [3]. However, there are two broad categories namely External Testing and BIST. The External Testing techniques include the methodologies based on Automatic Test Pattern Generator (ATPG), Vector Reordering and architecture whereas the BIST include techniques based on LFSR, Test Scheduling, Circuit Partitioning and Reseeding.

However, the vector ordering can be used in BIST environment as well. In ordering techniques, the THD i.e. the sum of the hamming distances is minimized by modifying the order in which test vectors of a given test sequence are shifted into the CUT. The Travelling Salesman Algorithm (TSA) has been quite useful for ordering the test vectors. The test vector ordering has been useful in minimizing the hamming distance among test vectors and thereby reducing in average and peak power. [5] [7].

Reordering of test vectors does not affect the fault coverage as overall the same set of test vectors are applied, just their order is modified [6]. The paper [7] discussed about two methods used for reordering of test vectors in order to reduce the dynamic power dissipation during testing of combinational circuits. Two search methods, 2-opt heuristic and a genetic algorithm based approach has applied and results obtained for combinational circuits. These techniques can be applied during external testing or deterministic BIST as well.

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III. MOTIVATION

Motivation for the proposed work arises from two observations. First is that the literature available focuses upon ordering the test vectors after obtaining the test vector sequences form the LFSR. And other is LFSR can itself be power efficient if modified for the purpose.

The aim of the work is to design an LFSR which in itself is power efficient and the test vectors generated from it are also power efficient. That is the test vectors cause lesser switching when scanned in.

IV. PROPOSED METHODOLOGY

In the proposed approach, an LFSR has been designed such that it reorders the test vectors to minimize the switching activity and consumes little power as compared to conventional LFSR.

The switching units (flip-flops) of the LFSR toggle unnecessarily in the process of generating $2^n$ sequence when same bits are repeated for a particular set of test sequences. Therefore the non performing flip-flops are disabled for a particular time period. The flip-flops are disabled by asserting the clock signal to state ‘0’. The behavior of the switching unit is projected in the Table 1.

<table>
<thead>
<tr>
<th>Data_in</th>
<th>Data_out</th>
<th>Clock</th>
<th>Modified clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The truth table logic can be realized by the use of an XOR and a NOR gate as shown in the figure 1.

\[
\text{THD} = \sum_{i=0}^{2^n-1} D(V_i, V_{i+1})
\]

The CL logic shown in figure 1 can be used with each LFSR cell without modifying its tap sequence and thus without changing its behavior. Thus the clock signal is modified in order to reduce power consumption.

Let the hamming distance test vector $V_i$ and $V_{i+1}$ be $D(V_i, V_{i+1})$ which is the total number of changes between the vectors $V_i$ and $V_{i+1}$. Then the Total Hamming Distance (THD) [9] can be calculated from the Equation (1)

<table>
<thead>
<tr>
<th>Test Vectors</th>
<th>Test vectors from Conventional LFSR</th>
<th>Reordered Test Vectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1</td>
<td>0 1 1</td>
<td>1 0 1</td>
</tr>
<tr>
<td>V2</td>
<td>0 0 1</td>
<td>0 0 1</td>
</tr>
<tr>
<td>V3</td>
<td>1 0 0</td>
<td>1 0 0</td>
</tr>
<tr>
<td>V4</td>
<td>0 1 0</td>
<td>0 1 0</td>
</tr>
<tr>
<td>V5</td>
<td>1 0 1</td>
<td>0 1 1</td>
</tr>
<tr>
<td>V6</td>
<td>1 1 0</td>
<td>1 1 0</td>
</tr>
<tr>
<td>V7</td>
<td>1 1 1</td>
<td>1 1 1</td>
</tr>
<tr>
<td>THD</td>
<td>10</td>
<td>9</td>
</tr>
</tbody>
</table>

New order of test vectors:

V5 $\rightarrow$ V2 $\rightarrow$ V3 $\rightarrow$ V4 $\rightarrow$ V1 $\rightarrow$ V6 $\rightarrow$ V7
V. PROPOSED ARCHITECTURE

Based on the suggested bit interchanging methodology, the modified LFSR can be designed using the conventional LFSR and a group of two-input multiplexers where bit n is considered as the selection line of the multiplexers. The architecture for interchanging the bits as per the proposed methodology is presented in figure 2.

Fig. 2 Architecture of Bit Interchanging Module.

In the figure, a case of odd n is considered. When n is even the interchanging is performed up to third and forth last FF outputs. Embedding the Bit Interchanging Module with the modified clock LFSR makes the design more power efficient as in Figure 3.

Fig. 3 Proposed general Modified TPG Architecture.

In this architecture the CL block contains the XOR and NOR logic for controlling the clock as shown in Figure. 1. The output from the LFSR is passed to the bit inter-changing module which constitutes of multiplexers. It interchanges the bits as per the proposed methodology and finally generates a set of reordered test vectors.

V. EXPERIMENTS AND ANALYSIS

In order to analyze the power reduction from the proposed TPG architecture, we have evaluated the power consumption in 8 bit conventional LFSR and 8 bit LFSR with modified clock for same input vector and same clock cycles. Experiments were performed Xilinx ISE 9.2i platform and total power consumption was calculated using Xpower. The result of Table 3, shows that the disabling the flip-flops for a time period when they are not performing, leads to reduction in total power consumption up to 10%.

A MATLAB program is written which generates bit-interchanged test vectors. These test vectors are actually the same but their order of scan shifting changes. The THD reduction obtained with maximal length LFSRs is presented in Table 4.

To predict the power efficiency of the test vectors, Weighted Transition Activity (WTA) was calculated. We used the weighted transition metric (WTM) [7] to predict power consumption due to scan vectors. Power estimation models have been presented in [8]. Consider a scan chain of length l and a scan vector $t_j = t^{*}_{j,1} t^{*}_{j,2} \ldots t^{*}_{j,k}$ with $t^{*}_{j,1}$ scanned in before $t^{*}_{j,2}$ and so on. For n vectors $t_1, t_2, t_3 \ldots t_n$ the average power ($P_{avg}$) is estimated as follows:

$$P_{avg} = \frac{\sum_{j=1}^{n} \sum_{i=1}^{l-1} (t_{j,i} \oplus t_{j,i+1})}{n}$$

To compare the average power consumption between a conventional LFSR and the Proposed LFSR, we calculated the WTA and thereafter $P_{avg}$ from the Equation (2). We used test vectors generated from 4bit, 8 bit, 12 bit and 16 bit maximal length LFSRs. The obtained results have been shown in Table 5.

<table>
<thead>
<tr>
<th>LFSR bits</th>
<th>Avg_power (Conventional LFSR)</th>
<th>Avg_power (Proposed LFSR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-bits</td>
<td>3.2000</td>
<td>2.7333</td>
</tr>
</tbody>
</table>
The obtained results from Table 5 show the decrease in average power calculated on the basis of weighted transition activity. The reduction in average power depends upon the tap sequences of the maximal length LFSR. Two approaches for indicating the reduction in power consumption viz. THD based prediction and WTM based prediction have been used.

V.III. CONCLUSION

The proposition is an attempt to invoke research on the test pattern generator itself. The techniques available so far have focused upon reducing the switching activity from the test patterns generated from the generator. Embedding the switching activity minimizing techniques with a power efficient test pattern generators will be a good step ahead. Therefore a modification is proposed in the conventional LFSR by embedding it with control logic module and bit interchanging module. This culminates into a novel architecture of the test pattern generator (TPG). The modified TPG architecture is capable of not only disabling the switching units for a particular time frame but also reorders the test vectors so as to reduce the transition activity. The benefit of the proposed TPG is that it can be used with any other low power technique to have further reduction in power.

REFERENCES