The aim of this paper is to propose a third order current-mode oscillator, based on DDCC and VDTA. The features of the proposed circuits are that the oscillation condition can be adjusted independently from the oscillation frequency by electronic method. The circuit construction consists of 1 DDCC, 1 VDTA, 1 grounded resistor and 2 grounded capacitors. The PSPICE simulation results are also shown, which are in correspondence with the theoretical analysis.

II. THEORY AND PRINCIPLE

A. Basic Concept of DDCC

The electrical behaviors of the ideal DDCC are represented by the following hybrid matrix [15]:

\[
\begin{bmatrix}
V_x \\
I_1 \\
I_2 \\
I_3 \\
I_Z
\end{bmatrix} =
\begin{bmatrix}
0 & 1 & -1 & 1 & 0 \\
0 & 0 & 0 & 0 & V_x \\
0 & 0 & 0 & 0 & V_z \\
0 & 0 & 0 & 0 & V_x \\
1 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
V_x \\
I_1 \\
I_2 \\
I_3 \\
I_Z
\end{bmatrix}.
\]

(1)

The symbol and the equivalent circuit of the DDCC are illustrated in Fig. 1(a) and (b), respectively.

![DDCC Symbol and Equivalent Circuit](image)

B. Basic Concept of VDTA

The circuit symbol of VDTA is shown in Fig. 2, where \(V_p\) and \(V_n\) are the input terminals, \(Z\) and \(X\) are the output ones. Hence, \(Z\) is the current output terminal; current through \(Z\)
terminal follows the difference of the voltages at \( V_P \) and \( V_N \) terminals by transconductances \( g_{m1} \). The voltage \( v_z \) on \( Z \) terminal is transferred into current using transconductance \( g_{m2} \), which flows into output terminal \( X \). The \( g_{m1} \) and \( g_{m2} \) are tuned by \( I_{B1} \) and \( I_{B2} \), respectively. In general, CDTA can contain an arbitrary number of \( x \) terminals, providing currents \( I_X \) of both directions. All terminals of VDTA exhibit high impedance values [17]. The characteristics of the ideal VDTA are represented by the following hybrid matrix:

\[
\begin{bmatrix}
I_{x} \\
I_{X} \\
I_{X-}
\end{bmatrix}
= 
\begin{bmatrix}
g_{m1} & g_{m1} & 0 \\
0 & 0 & g_{m2} \\
0 & 0 & g_{m2}
\end{bmatrix}
\begin{bmatrix}
V_{P} \\
V_{N} \\
V_{Z}
\end{bmatrix}.
\tag{2}
\]

If the VDTA is realized using CMOS technology, \( g_{m1} \) and \( g_{m2} \) can be respectively written as

\[g_{m1} = \sqrt{kI_{B1}},\tag{3}\]

and

\[g_{m2} = \sqrt{kI_{B2}}.\tag{4}\]

Here \( k \) is the physical transconductance parameter of the CMOS transistor. \( I_{B1} \) and \( I_{B2} \) are the bias current used to control the \( g_{m1} \) and \( g_{m2} \), respectively.

From Eq. (5), the condition of oscillation (OC) and frequency of oscillation (FO) can be written as

\[OC : ab = ck\tag{6}\]

and

\[\omega_{oc} = \sqrt{a}\tag{7}\]

From Eq. (5), if \( a = c \), the oscillation condition and oscillation frequency can be adjusted independently, which are the oscillation condition can be controlled by \( b \) and \( k \), while the oscillation frequency can be tuned by \( a \).

D. Proposed Oscillator

The completed 3rd current-mode quadrature oscillator is shown in Fig. 4. The condition of oscillation and frequency of oscillation can be written as

\[\frac{1}{C_1R} = \frac{g_{m2}}{C_3},\tag{8}\]

and

\[\omega_{oc} = \sqrt{\frac{g_{m2}}{C_1C_3R}}.\tag{9}\]

It is obviously found that, the condition of oscillation and frequency of oscillation can be adjusted independently, which are the oscillation of oscillation can be controlled by setting.
The phase difference $\phi$ between $I_{o1}$ and $I_{o2}$ is $\phi = -90^\circ$ ensuring that the currents $I_{o2}$ and $I_{o1}$ are in quadrature.

### III. RESULTS OF COMPUTER SIMULATION

The working of the proposed oscillator has been verified in PSpice simulation. Internal constructions of DDCC and VDTA used in simulation are respectively shown in Figs. 5 and 6. The PMOS and NMOS transistors have been simulated by respectively using the parameters of a 0.25µm TSMC CMOS technology [16]. The transistor aspect ratios of PMOS and NMOS transistor are indicated in Table I. The circuit was biased with $\pm 1.25$V supply voltages, $V_{BB}=-0.55V$, $C_1=C_2=C_3=50pF$, $I_{B1}=I_{B2}=60\mu A$ and $R=3.5k\Omega$. This yields simulated oscillation frequency of 1MHz. Fig. 7 shows simulated quadrature output waveforms. Fig. 8 shows the simulated output spectrum, where the total harmonic distortion (THD) is about 2.95%. The quadrature relationship between the generated waveforms has been verified using Lissagous figure and shown in Fig. 9. The power consumption is approximately 1.76mW.

#### TABLE I

**DIMENSIONS OF THE TRANSISTORS**

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width (µm)</th>
<th>Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$-$M_4$</td>
<td>3</td>
<td>0.25</td>
</tr>
<tr>
<td>$M_5$-$M_8$</td>
<td>1</td>
<td>0.25</td>
</tr>
<tr>
<td>$M_9$-$M_{10}$</td>
<td>10</td>
<td>0.25</td>
</tr>
<tr>
<td>$M_{11}$-$M_{12}$, $M_{13}$-$M_{16}$</td>
<td>5</td>
<td>0.25</td>
</tr>
<tr>
<td>$M_{17}$-$M_{20}$</td>
<td>8</td>
<td>0.25</td>
</tr>
</tbody>
</table>

### IV. CONCLUSION

A 3rd current-mode quadrature sinusoidal oscillator based on DDCC and VDTA has been presented. The features of the proposed circuit are that: oscillation frequency an oscillation condition can be orthogonally adjusted via input bias current; it consists of 1 DDCC, 1 VDTA, 1 grounded bias resistor and 3 grounded capacitors, which is convenient to fabricate. The PSpice simulation results agree well with the theoretical anticipation.

#### REFERENCES


