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Decimation Filter Design Toolbox for Multi-Standard Wireless Transceivers using MATLAB

Shahana T. K., Babita R. Jose, K. Poulose Jacob and Sreela Sasi

***Abstract*—**The demand for new telecommunication services requiring higher capacities, data rates and different operating modes have motivated the development of new generation multi-standard wireless transceivers. A multi-standard design often involves extensive system level analysis and architectural partitioning, typically requiring extensive calculations. In this research, a decimation filter design tool for wireless communication standards consisting of GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX is developed in MATLAB® using GUIDE environment for visual analysis. The user can select a required wireless communication standard, and obtain the corresponding multistage decimation filter implementation using this toolbox. The toolbox helps the user or design engineer to perform a quick design and analysis of decimation filter for multiple standards without doing extensive calculation of the underlying methods.

***Keywords*—**Decimation filter, MATLAB® toolbox, Multi-standard transceivers, Sigma-delta A/D converter.

I. Introduction

CURRENT radio frequency (RF) transceivers demand higher integration for low cost and low power operations, and adaptability to multiple communication standards. Specifically, software defined radio (SDR) is a wireless interface technology in which software-programmable hardware is used to provide flexible radio solutions in a single transceiver system. Multi-standard operation is achieved by using a receiver architecture that performs channel selection on chip at baseband [1]. This baseband channel filtering is performed in digital domain to adapt to the channel bandwidths, sampling rates, carrier to noise (C/N) ratio, and blocking and interference profiles of multiple communication standards [2]. Sigma-delta analog to digital converters (SD-ADCs) are used in multi-standard transceivers to adapt to the requirements of different standards. The dynamic range of a SD-ADC can be easily adjusted by selecting different oversampling ratios. The SD-ADC consists of a sigma-delta modulator and a decimation filter. Sigma-delta modulator based on oversampling technique provides high resolution over wide bandwidth that is required in multi-mode receivers. It also shifts the noise into high frequency keeping the signal to noise ratio (SNR) high in the signal band. The digital decimation filter selects a desired channel and removes the out-of-band quantization noise produced by the modulator. Further, it reduces the sampling rate from oversampled frequency of the modulator to the Nyquist rate of the channel [3]. Therefore in a multi-mode transceiver, SD-ADC requires a decimation filter with programmable decimation ratios.

Several papers are available in literature that deals with the design issues of decimation filters for wireless communication transceivers. A fifth order comb decimation filter with programmable decimation ratios and sampling rates for GSM (Global System for Mobile communications) and DECT (Digital Enhanced Cordless Telecommunication) standards are presented in [4]. The design and implementation of digital filter processors that can be used as downsamplers in wireless transceivers is detailed in [5]. A low complexity decimation filter architecture is presented in [6] by using infinite impulse response (IIR) filters implemented by all-pass sum that avoids multiplications. A low-power high linearity variable gain amplifier (VGA) embedded in a multi-standard receiver that meets the standard requirements is reported in [7]. Decimation filter design for GSM, WCDMA (Wideband Code Division Multiple Access), 802.11a, 802.11b, 802.11g and WiMAX (Worldwide Interoperability for Microwave Access) standards are given in [8]. Multi-rate digital filters and fractional frequency conversion techniques are adopted to implement the front end of a dual-mode receiver for WCDMA/cdma2000 in [9]. A decimation filter structure based on cascaded integrator comb (CIC) filters and polynomial interpolation filters to perform fractional sample rate conversion is presented in [10].

In this paper, a decimation filter design toolbox is developed in MATLAB® GUIDE (Graphical User Interface Development Environment) addressing the design issues presented in the above papers. The toolbox includes six wireless standards given in [8], and provides an appropriate multistage decimation filter for each standard. Decimation is done in two or three stages to reduce the hardware complexity and power dissipation. Each stage is implemented with optimized filters so that the overall cascaded filter response meets the specification for a particular standard. The implementation complexity in terms of filter length that meets the specification for any of these standards is computed using this tool, and is tabulated. The rest of the paper is organized as follows: Section II describes the receiver architecture and the sigma-delta modulator suitable for multi-standard operation. Section III presents a multistage decimation filter structure

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with design specification for each standard. The type of filters used for implementing each stage is also described. Section IV describes the GUI (graphical user interface) and its features for the toolbox. Section V provides the decimation filter implementation results for multiple standards. Finally, Section VI concludes the paper.

II. Receiver Architecture for Multi-standard Operation

This section deals with the receiver architecture which emphasizes high integration and multi-standard capability [11], [12]. High integration can be achieved by utilizing a receiver architecture that performs baseband channel select filtering on chip. This enhances the programmability to different dynamic range, linearity and signal bandwidth to meet the requirements of multiple RF standards. A wideband high dynamic range sigma-delta modulator can be used to digitize both the desired signal and potentially stronger adjacent channel interferers.

Fig. 1 shows a direct conversion homodyne architecture [2] which is an example of a receiver suitable for high integration and adaptability. It is also known as zero-IF receiver. This architecture translates frequency to baseband directly to eliminate external components within the receive path. It can be programmed for a multi-standard solution since the local oscillator (LO) is tuned to the same frequency as the incoming RF frequency to select different standards. On the other hand, a DC offset is created at the output of the mixer. Here, the incoming RF signal is multiplied by one sided LO signal of a frequency equal to the centre frequency of the desired signal band, and hence does not suffer from image signal interference. The downconversion with a one sided LO signal is achieved by a quadrature mixer in which the incoming signal is multiplied by two LO signals with 90 degrees out of phase. These in-phase and quadrature phase components are then lowpass filtered and sent to ADCs. The digital signal from ADC is given to digital signal processing section for demodulation. Homodyne receivers are multi-standard capable because the channel filtering is done at baseband. However, the noise and DC offset are to be reduced to achieve adequate dynamic range.

The sigma-delta ($\sum\Delta$) analog-to-digital converters (ADCs) are widely used in wireless systems because of their superior linearity, robustness to circuit imperfections, inherent resolution-bandwidth trade off and increased programmability in digital domain. A highly linear sigma-delta modulator for multi-standard operation that can achieve high resolution over a wide variety of bandwidth requirements remains challenging. A reconfigurable ADC [11], [12] is a promising solution to keep the power dissipation as low as possible.

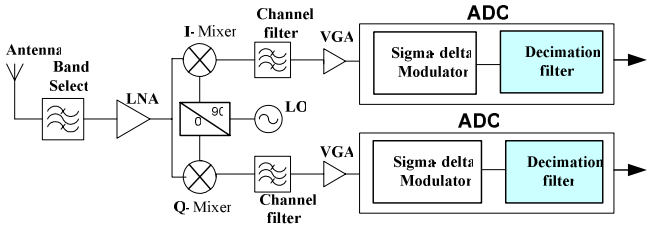


Fig. 1 Direct conversion homodyne receiver architecture

Single loop and multistage noise shaping (MASH) topologies are two different approaches for implementing $\sum\Delta$ modulators. Single loop structures with a higher-order noise transfer function combined with multi-bit feedback can achieve higher dynamic range (DR) with low oversampling ratio (OSR). But the linearity and resolution of the overall $\sum\Delta$ modulator are limited by the precision of the multi-bit DAC. MASH topology is preferred over single loop structures since the coefficients are optimized for a specific OSR. It has flexibility to handle different OSRs with little modification. MASH structures can be adopted for multi-mode receivers considering the stability and reconfigurability.

The theoretical dynamic range has been used in conjunction with the implementation attributes to choose the optimal topology for different RF standards. The dynamic range DR of a $\sum\Delta$ modulator is given by (1),

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} M^{2L+1}(2^B - 1)^2 \quad (1)$$

where L is the order of the modulator, M is the oversampling ratio (OSR), and B is the number of bits of the quantizer. The six popular standards considered in this paper are GSM, WCDMA, 802.11a, 802.11b, 802.11g and WiMAX. These standards have different bandwidth requirements. Since the bandwidth requirements of WLAN-a, b, g and WiMAX are more or less the same, the same topology can be adopted with different oversampling ratios (OSRs). This will reduce the DR calculation for the main three standards GSM, WCDMA and WLAN (Wireless Local Area Network) whose dynamic range requirements are chosen to be 94dB, 79dB and 69dB respectively.

OSR can be selected as 128 for low data rate application, such as GSM receiver, due to a much smaller signal bandwidth. A basic second order modulator with 1-bit quantization is sufficient for this kind of application. In order to meet the DR requirements demanded by the WCDMA standard, a fourth order cascaded MASH topology will be enough with an OSR of 16. If WLANa becomes the target standard, a fifth order topology is a good compromise to achieve the required DR with a 4-bit quantizer and an OSR of 8. The sigma-delta modulator can be made programmable, and all the blocks are switched to operation only in the WLAN mode. This results in power saving when the receiver is operating in other modes. Similar considerations apply for other standards also. The OSR is chosen as 12, 12 and 8 for WLANb, WLANg and WiMAX respectively. Sigma-delta modulator is followed by a programmable decimation filter

operating in the digital domain. The proposed work focuses on the design of multistage decimation filter for multiple standards, which is highlighted in Fig. 1.

III. Multistage Decimation Filter

The sampling rate is downconverted from the oversampled rate of sigma-delta modulator to a data rate that can be conveniently processed by existing DSP processors. This minimizes the power consumption of DSP processors for demodulation and equalization. The purpose of decimation filter is to remove all the out-of-band signals and noise, and to reduce the sampling rate from oversampled frequency of the sigma-delta modulator to Nyquist rate of the channel. The decimation filter consists of a lowpass filter and a downsampler. It is possible to perform noise removal and downconversion with a single FIR filter. The filter order N of FIR lowpass filter is given in (2), where D_∞ is a function of the required ripples δ_p and δ_s in the passband and stopband respectively, F_s is the sampling frequency and Δf is the width of transition band.

$$N \approx D_\infty\left(\delta_p, \delta_s\right)\left(\frac{F_s}{\Delta f}\right) \tag{2}$$

As the sigma-delta modulators are oversampled, the transition band is small relative to sampling frequency leading to excessively large filter orders. The power consumption of the filter depends on the number of taps as well as the rate at which it operates. So computational complexity is high for single stage implementation of decimation filter and consumes much power. This can be overcome by multistage approach.

Implementing decimation filter in several stages reduces the total number of filter coefficients. The filters operating at higher sampling rates have larger transition bands, and the filters with lower transition bands operate at reduced sampling frequencies. Subsequently, the hardware complexity and computational effort are reduced in multistage approach. This will lead to low power consumption. A multistage sampling rate conversion (SRC) system consists of a cascade of single stage SRC systems as shown in Fig. 2. The 'i^{th}' stage performs decimation by a factor of 'R_i' such that the overall decimation factor 'R' is given by $R = \prod_{i=1}^{P} R_i$, where 'P' is the total number of stages. The individual filter of each stage is designed within the frequency band of interest in order to prevent aliasing in the overall decimation process.

The performance of a decimation filter depends on the filter architecture and the order of each stage of a multistage decimator. FIR filters are widely used in decimators as most of the modulation schemes require linear phase characteristics. The different filter architectures used in this work are given below.

A. Filter Architectures

1) Cascaded Integrator Comb (CIC) filter

Hogenauer devised a flexible, multiplier free Cascaded Integrator Comb (CIC) filter that can handle large sampling rate changes suitable for hardware implementation [13]. The basic structure of the Hogenauer CIC filter is shown in Fig. 3. This consists of an integrator and a comb filter as two basic building blocks. So, it is an infinite impulse response (IIR) filter followed by a finite impulse response (FIR) filter. In a CIC filter of order k, the integrator section consists of a cascade of 'k' digital integrators operating at the high sampling rate F_s. Each integrator is a one-pole filter with unity feed back coefficient, and the transfer function is

$$H_I(z) = \frac{1}{1 - z^{-1}} \tag{3}$$

The comb section consists of 'k' comb stages with a differential delay of 'M' and operates at the low sampling rate F_s/R, where 'R' is the rate change or decimation factor. The transfer function of a comb stage referenced to high sampling rate is

$$H_C(z) = 1 - z^{-RM} \tag{4}$$

The rate change switch between the two filter sections subsamples the output of the integrator stage reducing the sample rate from F_s to F_s/R. In practice, the differential delay, M is usually held equal to 1 or 2. Using (3) and (4), the system transfer function of the CIC filter with respect to the high sampling rate F_s is given by

$$H(z) = H_I^k(z) H_C^k(z) = \frac{\left(1 - z^{-RM}\right)^k}{\left(1 - z^{-1}\right)^k} = \left[\sum_{i=0}^{RM-1} z^{-i}\right]^k \tag{5}$$

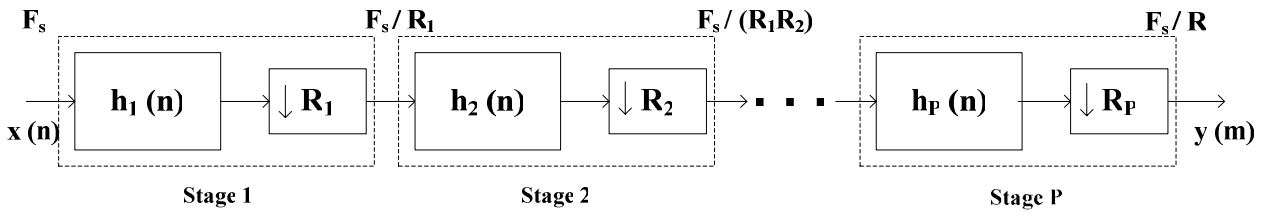


Fig. 2 Multistage decimation filter

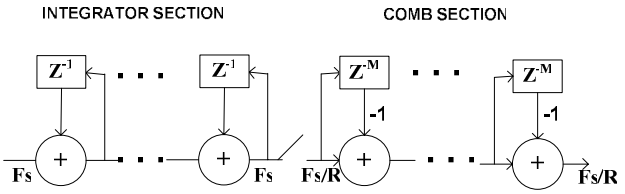


Fig. 3 CIC decimation filter

The working of CIC filters is based on the fact that perfect pole/zero cancellation can be achieved. From the transfer function in (5), it is clear that *RM* zeros are generated by the numerator term with a multiplicity of *k*. The *k* poles at z = 1, generated by the denominator are cancelled by the *k* zeros of the CIC filter [14]. On evaluating the frequency response given by (5) at $z = exp(j2\pi f/R)$, where '*f*' is the frequency relative to low sampling rate (F_s/R), the magnitude response of CIC filter is obtained as

$$\left|H(f)\right| = \left|\frac{\sin \pi M f}{\sin \frac{\pi f}{R}}\right|^N \tag{6}$$

As for small values of '*x*', $sinx \approx x$, the magnitude response given in (6) can be approximated for large '*R*' as

$$\left|H(f)\right| = \left|RM \frac{\sin \pi M f}{\pi M f}\right|^N \text{ for } 0 \le f < \frac{1}{M} \tag{7}$$

The output spectrum has nulls at multiples of $f = \frac{1}{M}$. The aliasing or imaging occurs in the region around the nulls. An example of CIC response used for GSM case, with F_s = 34.667 MHz, *R* = 32, *M* = 1 and *k* = 3 is shown in Fig. 4.

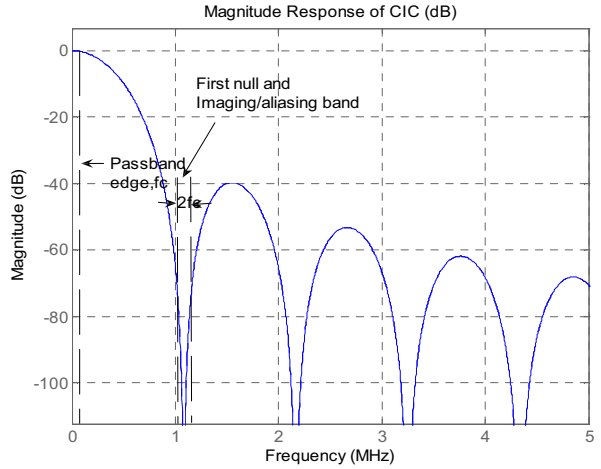


Fig. 4 CIC magnitude response for GSM with F_s = 34.667 MHz, *R* = 32, *M* = 1 and *k* = 3

The amount of passband aliasing or imaging error can be brought within prescribed bounds by increasing the number of stages in the CIC filter. It will also increase the passband droop. The width of the passband and the frequency characteristics outside the passband are severely limited. So, CIC filters are used only to facilitate transition between high and low sampling rates. The CIC filter is followed by one or two stages of finite impulse response (FIR) filters operating at low sampling rates. These are designed to attain the required transition bandwidth and stopband attenuation.

2) *Halfband filter*

Halfband filters are a special class of symmetric FIR filters used in second stage of multistage decimators. Halfband filters are characterized by equal passband and stopband ripples ($\delta_p = \delta_s$), and the transition band is symmetrical about π/2 such that $\omega_p + \omega_s = \pi$, where ω_p and ω_s correspond to the passband and stopband edges. The impulse response *h(n)* exhibits symmetry with almost 50% of coefficients 'zero' and with a magnitude of 0.5 at $F_s/4$. This implies reduced number of filter taps, lesser hardware and low power consumption. Halfband filters are used to perform decimation by a factor of 2 [3]. The ideal halfband filter characteristics is as shown in Fig. 5, where Δf is the width of the transition band and F_s is the sampling frequency.

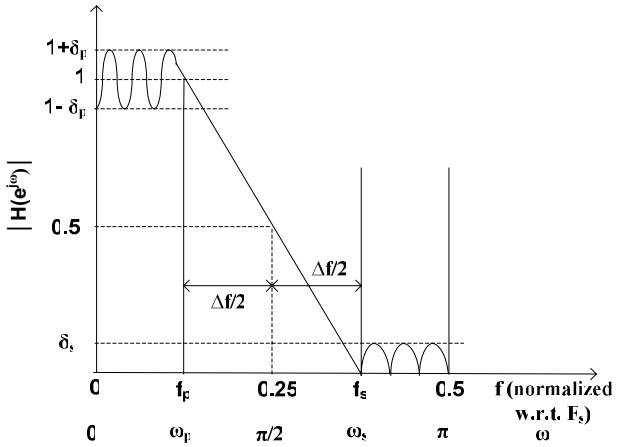


Fig. 5 Magnitude response of halfband filter

3) *FIR filter*

The third type of filter used in the multistage decimator is a FIR filter. The CIC filter response exhibits a droop in the passband which progressively attenuates the signals. The passband droop and stopband attenuation increases as the number of sections of CIC filters increases. The FIR filter used in the last stage performs decimation and CIC droop compensation. This FIR filter is designed according to the differential delay and number of sections of CIC filter along with the passband ripple and stopband attenuation to meet the overall specification of a particular standard. So, a low computational complexity multistage decimator for a required specification can be obtained with a CIC filter followed by halfband and droop correct FIR filter. The magnitude response of a droop compensating FIR filter designed to compensate the passband droop produced by a CIC filter with a differential delay of *M* = 1, and number of sections *k* = 4, is shown in Fig. 6.

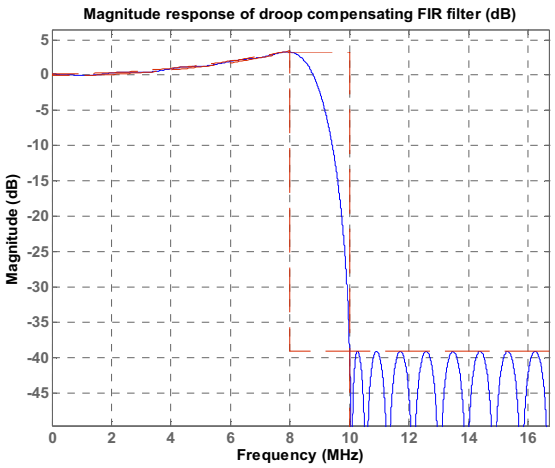


Fig. 6 Magnitude response of droop compensating FIR filter with $M = 1$ and $k = 4$

B. Decimation Filter Design Specification

The specifications for all six standards considered in this research and their corresponding decimation filter design parameters are given in Table I. The oversampling ratio (OSR) for each standard is selected so as to get the required dynamic range for the sigma-delta modulator of a particular order and number of quantizer bits. The receiver specifications and the blocking and interference profiles are defined first in order to set the parameters for the decimation filter. There are large undesired signals called 'blockers' within the same cell, and large undesired signals known as 'adjacent channel interferers' from the neighbouring cells. These interference signals are to be limited within a certain range for each standard for proper reception of the desired signals. The decimation filter is generally designed to minimize the undesired signals in the desired band of operation. The output carrier to noise (C/N) ratio is calculated from the bit error rate (BER) of each standard and the modulation scheme used. Table II gives the interference profile and the C/N ratio for all the six standards [8]. The passband frequency edge is taken as 80% of the bandwidth. The passband ripples are chosen to minimize signal distortions in the signal band. The stopband attenuations shown in Table I are selected according to the interference profile and C/N ratio given in Table II for each standard.

TABLE I
MULTI-STANDARD SPECIFICATIONS AND DECIMATION FILTER DESIGN PARAMETERS

Standards	Frequency range (GHz)	Channel Spacing (MHz)	Symbol rate / Chip rate	OSR	Input sampling frequency, F_s (MHz)	Pass band edge (MHz)	Stop band edge (MHz)	Passband ripple (dB)	Stopband attenuation (dB)
GSM	DL:0.935-0.96 UL:0.89-0.915	0.2	270.833 Ksymbols/s	128	34.667	0.08	0.1	0.1	65
WCDMA	DL:2.11-2.17 UL:1.92-1.98	5	3.84 Mchips/s	16	61.44	2	2.5	0.5	55
WLANa	5.15-5.35	20	12 Msymbols/s	8	96	8	10	0.5	44
WLANb	2.4-2.4835	25	11 Mchips/s	12	132	10	12.5	0.5	42
WLANg	2.4-2.4835	25	12 Msymbols/s	12	144	10	12.5	0.5	44
WiMAX	10-66	20	16.704 Msymbols/s	8	133.632	8	10	0.5	39

TABLE II
INTERFERENCE PROFILE AND C/N RATIO

Standard	Offset from central frequency(MHz) : Interference magnitude(dBm)				C/N ratio (dB)
GSM	0.2 : -90	0.4 : -58	0.6 : -46	1 : -42	9.7
WCDMA	5 : -63	10 : -56	12.5:-44		7.2
WLANa	20 : -63	40 : -47			28
WLANb	25 : -35				7
WLANg	20 : -63	40 : -47			28
WiMAX	20 : -68	40 : -49			21

IV. DECIMATION FILTER DESIGN TOOLBOX

The proposed 'Multistandard Decimation Filter Design Toolbox' is designed using the Signal Processing Toolbox and Filter Design Toolbox from MATLAB® using GUIDE environment. The user can select a required wireless

communication standard and obtain the corresponding multistage decimation filter implementation using this toolbox. The toolbox will help the user or design engineer to perform a quick design and analysis of a decimation filter for multiple standards without doing extensive calculation of the underlying methods. The front panel of the GUI is shown in Fig. 7 and the features of the toolbox are detailed below.

A. Multi-stage Decimation Filter Design

The toolbox is designed for six popular wireless communication standards, namely GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX. Initially, the desired standard is selected from the pop-up menu as in Fig. 8 and the filter design is obtained by pressing the push button named *Multistandard Decimation Filter Design*. The filter details such as the required channel spacing for a selected standard, passband edge, stopband edge, input sampling frequency, OSR, number of stages and type of filter used in each stage, decimation factors for each stage, and filter complexity are displayed on the GUI as in Fig. 9.

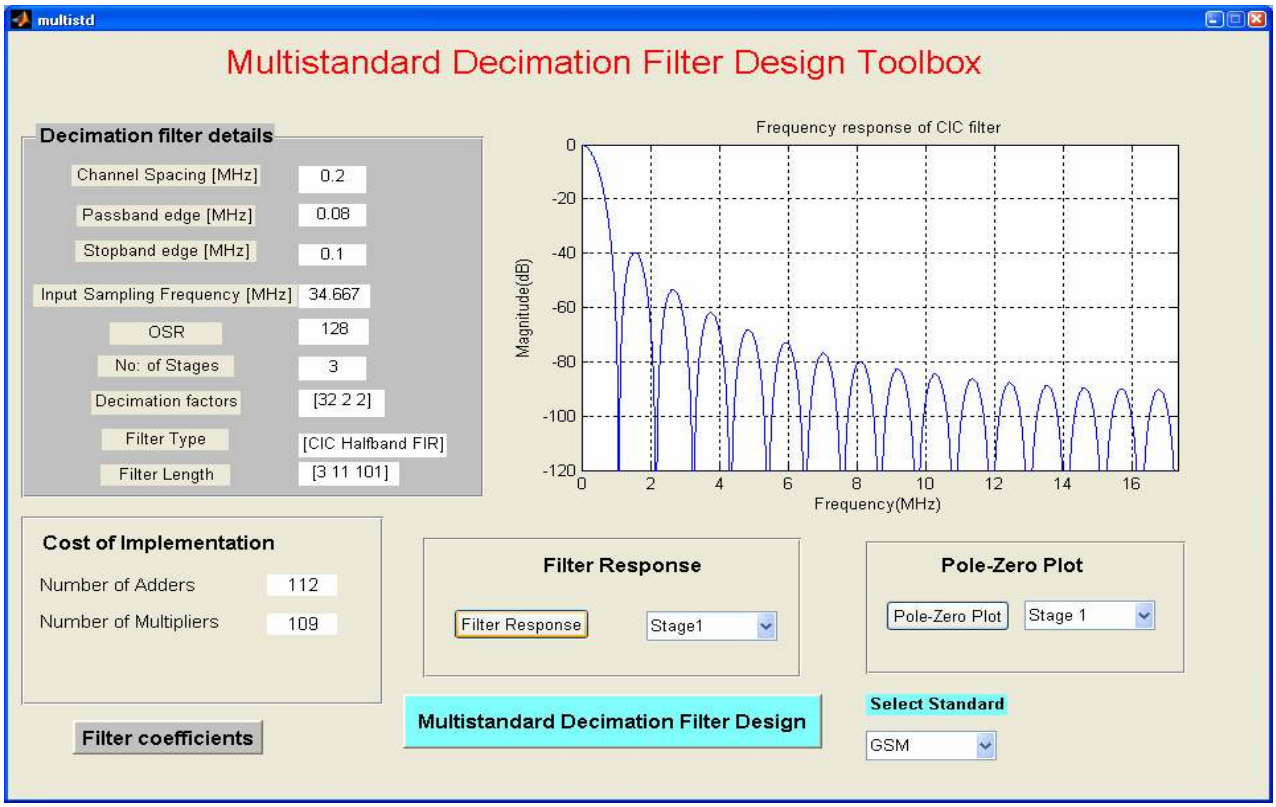


Fig. 7 The GUI for Multi-standard Decimation Filter Design Toolbox

Fig. 8 Pop-up menu for standard selection

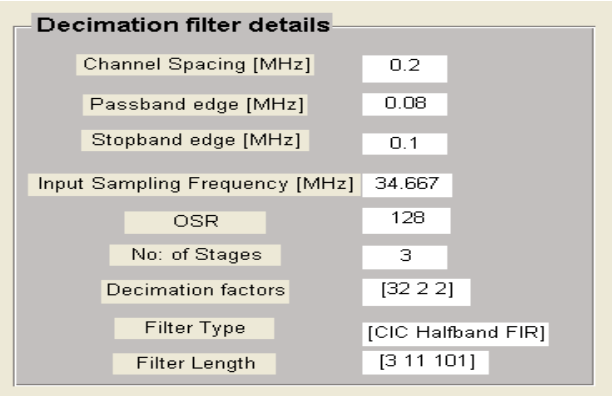


Fig. 9 Decimation filter details for GSM

B. Cost of Implementation

The cost of implementation of the multistage decimator is displayed as in Fig. 10, in terms of total number of adders and multipliers required for all stages.

C. Filter Co-efficients

The filter coefficients can be visualized by pressing the push button named *Filter coefficient*. Then a message box will pop up and it displays the filter coefficients for each stage. For GSM (current display), the message box displays the number of sections of the CIC filter as '3 integrators and 3 combs', 11 halfband filter coefficients and 101 droop compensation FIR filter coefficients, as shown in Fig. 11.

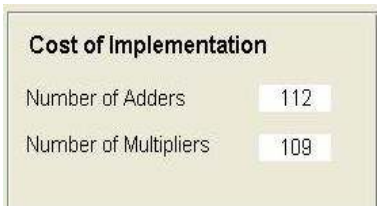


Fig. 10 Cost of decimation filter implementation for GSM

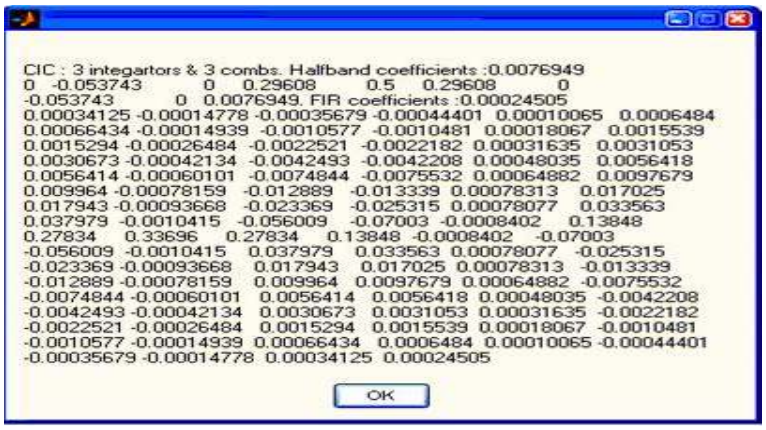


Fig.11 Message box displaying filter coefficients for GSM

D. Filter Response

The push button named *Filter response* is used to display the magnitude response. The desired response such as the magnitude response for individual filter stages, cascaded responses after each stage or the multistage overall response, can be selected from the pop-up menu as in Fig. 12. The cascaded filter response and the overall response of the multistage decimator are displayed using filter visualization tool (FVTool) in MATLAB as in Fig. 13. The magnitude response of individual filter is displayed on the graphical window, called axes, embedded on the front panel of the GUI as in Fig. 14.

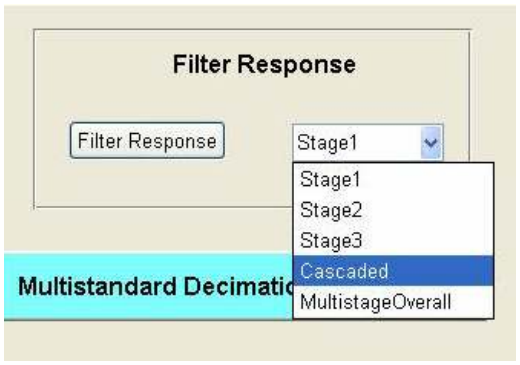


Fig. 12 Pop-up menu for magnitude response selection

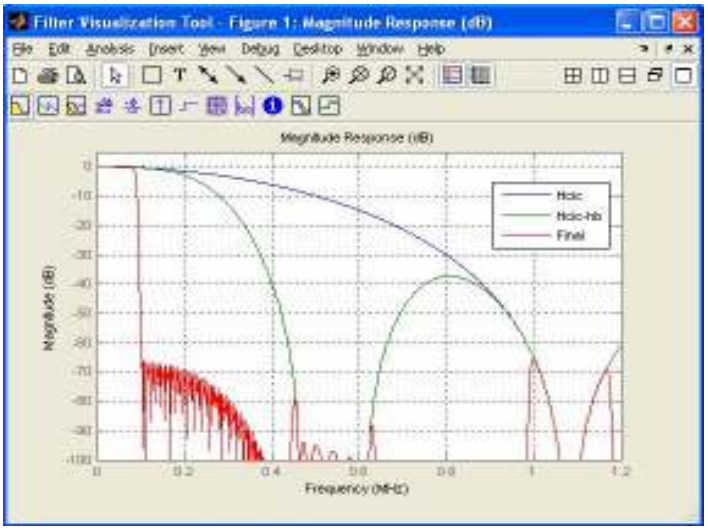
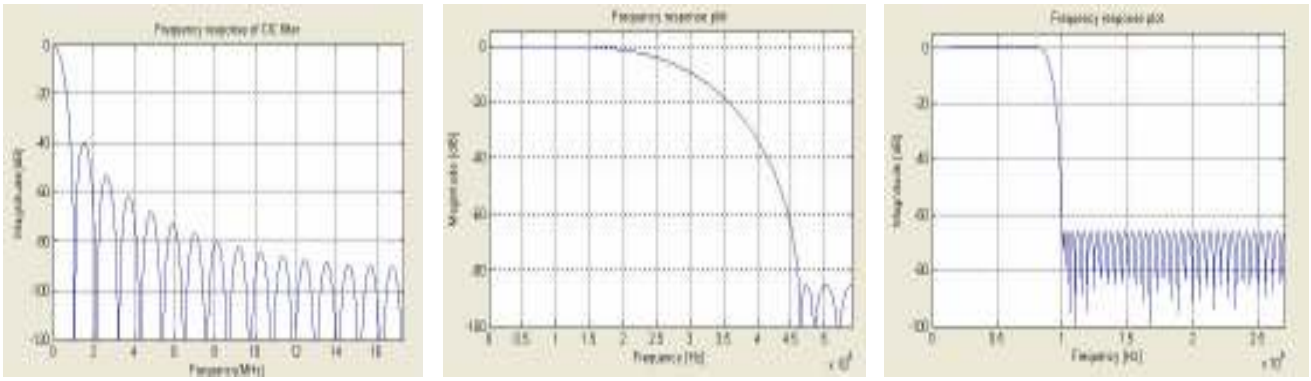


Fig. 13 Display of the cascaded filter response



(a) (b) (c)

Fig. 14 Individual Filter response for GSM displayed on front panel of GUI (a) CIC filter (b) Halfband filter (c) FIR filter

E. Pole-Zero Plots

To get the pole-zero plot of individual filter, each stage can be selected from a pop-up menu as in Fig. 15. The push button named *Pole-Zero Plot* is used to display the corresponding plot on the front panel graphical window of the GUI as in Fig. 16. The multiplicity number of each pole and zero are indicated in the plot. The filter is stable when the poles lie inside the unit circle in z-plane. FIR filters are stable by design since the transfer functions do not have denominator polynomials, and thus no feedback to cause instability. CIC filters are stable even with the presence of integrators, as the poles on unit circle due to the denominator of transfer function are cancelled by equal number of zeros at the same position produced by the numerator.

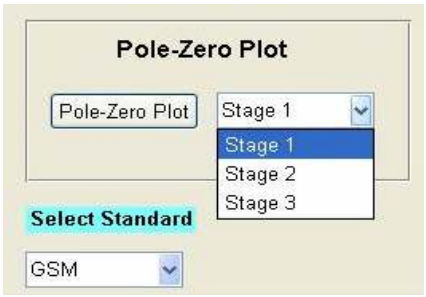


Fig. 15 Pop-up menu for pole-zero plots

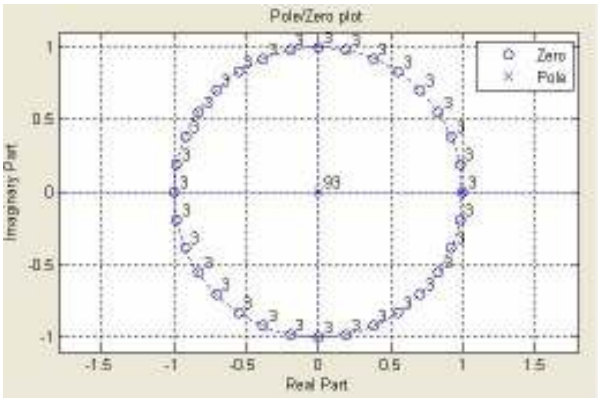


Fig. 16 (a)

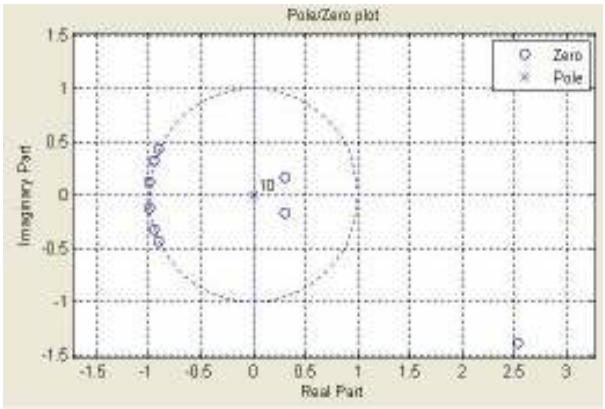


Fig. 16 (b)

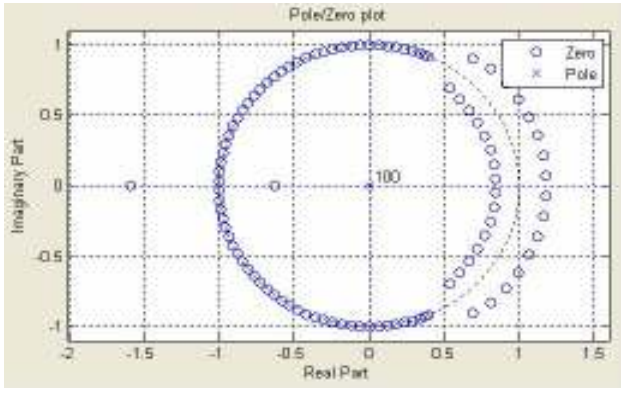


Fig. 16 (c)

Fig. 16 Pole-Zero plot of individual filters for GSM (a) CIC filter (b) Halfband filter (c) FIR filter

V. Decimation Filter Implementation and analysis

The individual stages of multistage decimation filter are designed to minimize hardware complexity as well as computational effort. For each stage, passband edge is same as 80% of the channel bandwidth, and stopband edge is selected to reduce the filter complexity while meeting the overall standard specification. The first stage, being a CIC filter, reduces the hardware as it consists of only adders and registers. But it exhibits passband droop and insufficient attenuation in the stopband. So the following filters are designed to compensate for the droop and to meet the overall filter specification for a particular standard. For GSM and WCDMA the second stage is selected as a halfband filter which has almost half the coefficients as 'zero'. The complexity of halfband filter is reduced by allowing a symmetrical transition band about $F_s/4$, where F_s is the sampling frequency at halfband input. So the stopband edge is relaxed for halfband filter. The third stage is a FIR filter that performs decimation as well as droop compensation in the passband. A three stage decimation filter is implemented for GSM and WCDMA. For WLANa, WLANb, WLANg and WiMAX decimation filter is implemented in two stages. The first stage is a CIC and the second stage is a CIC droop compensation FIR filter. The last stage of a decimation filter always has passband and stopband edges to meet the standard specification. Usually it will be more complex compared to the preceding stages, but operates at a reduced sampling frequency. Table III shows the decimation filter implementation details such as the type of filter used, the decimation factors, and the number of filter coefficients for each stage of all the six standards.

TABLE III
Decimation Filter Implementation Results for Multiple Standards

Standards	Modulator quantizer bits	OSR	Filter structure	Decimation factor	Filter length / No. of Sections
GSM	1	128	CIC	32	3
			Halfband	2	11
			FIR	2	101
WCDMA	1	16	CIC	4	4
			Halfband	2	19
			FIR	2	48
WLANa	4	8	CIC	4	9
			CIC compensation FIR	2	32
WLANb	4	12	CIC	4	7
			CIC compensation FIR	3	38
WLANg	4	12	CIC	4	6
			CIC compensation FIR	3	38
WiMAX	4	8	CIC	4	4
			CIC compensation FIR	2	36

VI. Conclusion

This paper presents a toolbox for the design of multistage decimation filter for six popular wireless standards namely GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX. The toolbox is developed using signal processing toolbox and filter design toolbox in MATLAB® using GUIDE environment. The user can select required wireless communication standard, and obtain the corresponding multistage decimation filter implementation using this toolbox. The toolbox will help the user or design engineer to perform a quick design and analysis of decimation filters for multiple standards without doing extensive calculation of the underlying methods. The tool provides the user with all necessary details of decimation filter designed for the selected standard including filter coefficients, frequency response, pole-zero plot etc. The tool will be made available to the public on request. The proposed implementation of multistage decimation filter reduces the hardware and computational effort while meeting the standard requirements. The OSR for each standard is selected to get the required dynamic range with a particular sigma-delta modulator order and number of quantizer bits. CIC is used as the first stage which is a simple structure consisting of only adders and registers. Using a halfband filter, with almost half the coefficients 'zero' in the next stage, provides further reduction in filter complexity. The last stage is a complex FIR filter which meets the overall standard specification but it operates at a reduced sampling frequency. The reduction in number of coefficients in each filter stage promises better synthesis results in terms of circuit compactness and power dissipation. Furthermore, it will be interesting to explore efficient multiple partitioning of the filter structure sharing common subsections of different standards. Multiple partitions may have different area/performance trade

off, and it may be possible to select an optimal granularity.

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