Decoder Design for a New Single Error Correcting/Double Error Detecting Code

M. T. Anwar, P. K. Lala, and P. Thenappan

Abstract—This paper presents the decoder design for the single error correcting and double error detecting code proposed by the authors in an earlier paper. The speed of error detection and correction of a code is largely dependent upon the associated encoder and decoder circuits. The complexity and the speed of such circuits are determined by the number of 1’s in the parity check matrix (PCM). The number of 1’s in the parity check matrix for the code proposed by the authors is fewer than in any currently known single error correcting/double error detecting code. This results in simplified encoding and decoding circuitry for error detection and correction.

Keywords—Decoder, Hsiao code, Parity Check Matrix, Syndrome Pattern.

I. INTRODUCTION

SINGLE bit error correcting and double-bit error detecting (SEC/DED) codes are widely used in computer memory systems. An SEC/DED code has a minimum Hamming distance of 4. One such code is the Hsiao code [1]. It uses multiple parity bits to uniquely identify an erroneous bit in a code word as well as to define the error-free condition.

In Hsiao’s code the columns corresponding to the information bits are assigned all combinations of 3-out-of-k bits, where k is the number of check bits; this is followed by all combinations of 5-out-of-k bits and then by 7-out-of-k bits and so on until all information bits have unique columns. The check bits are assigned l-out-of-k code words. The equations for the check bits in the PCM are derived by taking the linear sum (EX-OR) of all the information bits with 1s in a row in which the check bit is also a 1. A single bit error results in a syndrome pattern that matches a column of the PCM. Thus, matching a syndrome pattern to a column in the PCM can identify an erroneous bit. If the column corresponds to a check bit, then no correction is necessary. However, for maintenance purposes the error information is logged. Since the Hsiao code uses only odd number of 1’s in the columns of its PCM, a syndrome pattern corresponding to a single bit error has odd parity. If the syndrome has an even parity, the presence of a double bit error in a code word is indicated.

The speed of error detection and correction in a code is largely dependent upon the associated encoder and decoder circuits. The complexity and the speed of such circuits are determined by the number of 1’s in the parity check matrix (PCM). The fewer the number of 1’s in the PCM the less complex the encoding and decoding circuits are; fewer 1’s also enhance the speed of these circuits [2]. Among all the well-known SEC/DED codes the Hsiao code has the minimum number of 1’s in the PCM [3].

A new coding technique for single bit error correction and double bit error detection has been proposed in Ref.[4]. It differs from the Hsiao code in that columns are assigned m-out-of-k code where m ≤ k, with all combinations of 2-out-of-k chosen first followed by increased values of m till all columns get unique code words; it also appends to each column two residue bits that are set to the mod-3 residue of the number of 1’s in the corresponding column. Two columns are also incorporated, one for each residue bit. Each of the these columns is assigned a 1-out-of-(k+2) code word such that together with other assigned check bits they form a identity submatrix. The PCM for the proposed code is constructed as follows:

i. Assuming k check bits (c_k_1, c_k_2, . . . c_1, c_0) and two residue bits (r_1, r_0), a (k + 2)-bit column with a single 1 is assigned to the check bit c_i and residue bit r_j .

ii. If the length of the information bits is n and 1^c_2 ≤ n then n columns out of 1^c_2 are selected. If 1^c_2 = n , all 1^c_2 columns are selected.

iii. If 1^c_2 < n, all 1^c_2 columns are selected; the remaining columns are selected first from 1^c_3 columns, then from among 1^c_4 columns and so on. This process is continued till all n columns in the PCM have been specified.

iv. Append two bits to each column of the information bits by taking the mod-3 residue of the sum of the number of 1’s in the columns corresponding to the information bits. Every PCM column is treated as a binary number and the top most bit is considered as the least significant bit.

To illustrate let us assume 1^d_7d_6d_5d_4d_3d_2d_1d_0 = 11010000. The corresponding check/residue bits are r_f_r_g_r_h_r_i_r_j = 101010. The PCMs for other (n + k + 2, n) codes, where n is the number of information bits, can be derived in a similar manner. For example, the PCMs for the (41, 32) is shown in Fig. 1.
The error detection and correction strategy for a single bit error in a code word will result in the residual syndrome bits to be 11 if one of the corresponding columns in the PCM has 01 in the last two bits and the other one has 10.

**Lemma 1:** A double bit error composed of two erroneous information bits in a code word will result in the residual syndrome bits given that the first erroneous pattern only has \( s_j \) number of 1’s in its first \( k \) syndrome bits. In the absence of a possibility of two 1’s in the first \( k \) syndrome bits of the syndrome pattern, as noted in the third column using ‘NO’, the corresponding fourth column value is ‘n/a’.

<table>
<thead>
<tr>
<th>Number of Errors</th>
<th>Syndrome Bits</th>
<th>Possibility</th>
<th>m1m0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>YES</td>
<td>00</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>NO</td>
<td>n/a</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>YES</td>
<td>00</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>NO</td>
<td>n/a</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>YES</td>
<td>11</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>NO</td>
<td>n/a</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>YES</td>
<td>00</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>NO</td>
<td>n/a</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>NO</td>
<td>n/a</td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>YES</td>
<td>11</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>NO</td>
<td>n/a</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>YES</td>
<td>00</td>
</tr>
</tbody>
</table>

**Proof:** The mod-3 residue bits of a column in the PCM can only be 00 or 01 or 10 in the residual syndrome bits, \( m_i m_{0b} \), indicates a double or a multi bit error if the sum of 1’s of the first \( k \) syndrome bits of the syndrome pattern is exactly 2. The fourth column indicates the value of the residual syndrome bits given that there exists a possibility of two 1’s in the first \( k \) syndrome bits of the syndrome pattern, as noted in the third column using ‘NO’, the corresponding fourth column value is ‘n/a’. In the absence of a possibility of two 1’s in the first \( k \) syndrome bits of the syndrome pattern, the resulting residual syndrome bit is either 00 or 11 and not 10. Using Table I, it can be concluded that only single bit errors with two 1’s in the first \( k \) syndrome bits can have 10 in the residual syndrome bits.

Similarly, it can be shown that a syndrome pattern that does not have 01 or 00 at the residual syndrome bits indicates a double bit if the sum of 1’s of the first \( k \) syndrome bit is exactly 4 or 3, respectively.

A major advantage of the code in [4] is the number of 1’s in the PCM is fewer than that in the Hsiao code except when \( k = 16 \) or 32 in which case the number of 1’s is almost the same as in Hsiao code. Table II shows the comparison of the number of 1’s in the new code in Ref.[4] and the Hsiao code.

**Procedure for correcting single bit errors and detecting double bit errors in an encoded word based on the proposed coding technique is given below:**

- Calculate the syndrome \( s = (m_1m_0s_{b1} . . . s_0) \)
- If \( (s_{b1} . . . s_0) \) bits are all zero then there are no errors in the information/check bits of the word, exit. Else

**TABLE II**

<table>
<thead>
<tr>
<th>Number of Errors</th>
<th>Syndrome Bits</th>
<th>Possibility</th>
<th>m1m0</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>54</td>
<td>YES</td>
<td>56</td>
</tr>
<tr>
<td>32</td>
<td>103</td>
<td>YES</td>
<td>105</td>
</tr>
<tr>
<td>64</td>
<td>216</td>
<td>YES</td>
<td>202</td>
</tr>
<tr>
<td>128</td>
<td>481</td>
<td>YES</td>
<td>411</td>
</tr>
<tr>
<td>256</td>
<td>1050</td>
<td>YES</td>
<td>962</td>
</tr>
</tbody>
</table>
iii. Compute the mod-3 residue of the syndrome bits $s_{k-1} \ldots s_0$; identify these as $m_1'm_0'$.

iv. If $m_1m_0 \neq 00$ and $(s_{k-1} \ldots s_0)$ bits are all zero then Residue Bit Error (RBE) exists, exit.

v. If $m_1m_0 = 00$ and $(s_{k-1} \ldots s_0)$ bits contain only a single 1, a check bit (CBE) identified by the syndrome pattern is erroneous, exit.

vi. If $m_1m_0 = 01$ and $m_1'm_0' = 01$ and the number of 1’s in the first $k$ syndrome pattern equals 3, a single bit error (SBE) is identified, decode.

vii. If $m_1m_0 = 01$ and $m_1'm_0' = 01$ and the number of 1’s in the first $k$ syndrome pattern equals 4, a single bit error (SBE) is identified, decode.

viii. If $m_1m_0 = 10$ and $m_1'm_0' = 10$ and the number of 1’s in the first $k$ syndrome pattern equals 2, a single bit error (SBE) is identified, decode.

ix. There is a double bit error (DBE) in the code word, exit.

II. DECODER DESIGN FOR THE PROPOSED CODE

A block diagram of the decoder circuit is shown in Fig. 2. The inputs to decoder are original information/check/residue bits and output is corrected information bits in the presence of a single bit error. In the case of no error / check bit error / residue bit error / double bit error, the information bits go through the decoder without correction. The decoder consists of the following:

A. Syndrome Bit Generator (SBG)

The syndrome bits $m_1m_0s_{k-1} \ldots s_0$ are calculated by EX-ORing the stored check/residue bits with the recomputed check/residue bits from information bits. The SBG only uses 2-input EX-OR gates and the total gate count, $SBG_c$, depends on the total number of 1’s in the PCM, $T$. The relationship between the $SBG_c$ and $T$ is as follows:

$$SBG_c = T - (k + 2)$$

where $k$ is the total number of check bits. The output of the SBG, syndrome bits $m_1m_0s_{k-1} \ldots s_0$, are later used by the No Error Detector block, the 1’s Counter block and the Single Bit Error Locator block. Note that the first $k$ syndrome bits, $s_{k-1} \ldots s_0$, are computed using original and recomputed check bits and the residual syndrome bits, $m_1m_0$, use original and recomputed residue bits, $r_{1f0}$.

B. No Error Detection (NED)

Using the first $k$ syndrome bits from the SBG the absence of errors can be identified. The NED block consists of only 2-input NOR gates and will output a 1 only if all $k$ syndrome bits are 0’s.

C. 1’s Counter (Counter)

This block counts the number of the 1’s in the first $k$ syndrome bits from the SBG block using only Half Adders. The output is a binary representation of the number of 1’s in the first $k$ syndrome bits.

D. 1’s Signal Generator (SG)

Using the output from the 1’s Counter, the SG block assigns individual outputs to binary representations of one, two, three, or four. To convert a binary representation of $x$ bits to a single output, only $(x - 1)$ 2-input gates are needed. Thus the outputs of the SG block are 1-1, 2-1, 3-1, and 4-1; in other words one-1, two-1’s, three-1’s, and four-1’s, respectively. During normal operation, only one output can be active at any given time.

E. MOD-3 Generator (M3G)

The MOD-3 Generator block also uses the output from the 1’s Counter to compute the mod-3 residue of the sum of 1’s in the first $k$ bits of syndrome pattern, and these are denoted as $m_1'm_0'$. For $7 < k < 16$, only two 2-input EX-OR gates are needed. The proposed code uses these outputs in the Error Identifier block to primarily identify double bit errors.

F. Error Identifier (EI)

The EI block identifies the type of error or no error during each memory read cycle. The inputs to the EI block include the output from the NED block, the output from the SG block, the outputs from the M3G block, along with $m_1$ and $m_0$. The outputs from the EI block are: Single Bit Error (SBE), Check Bit Error (CBE), and Residue Bit Error (RBE), as shown in Table III.
All other combinations yield a Double Bit Error (DBE) and this is the final output of the EI block. In Table III, x denotes don’t care. A SBE is present when any of the following conditions are met:

i. \( m_1 = 0, m_0 = 0, m_1' = 0, m_0' = 0 \) and \( 3-1 = 1 \) or,
ii. \( m_1 = 0, m_0 = 1, m_1' = 0, m_0' = 1 \) and \( 2-1 = 1 \) or,
iii. \( m_1 = 1, m_0 = 0, m_1' = 1, m_0' = 0 \) and \( 4-1 = 1 \).

A CBE output is 1 when the first \( k \) bits of the syndrome has only one 1. The RBE identifies errors in the residue bits and becomes 1 whenever either \( m_0 \) or \( m_1 \) is 1 in the presence of no error. The EI block is implemented using twenty two 2-input gates and 5 inverters.

G. Single Bit Error Locator (SBEL)

This block is responsible for locating the erroneous bit based on the syndrome bits. The SBEL block identifies the syndrome bit in the presence of a SBE using the all bits of the syndrome. It consists of 2-input EX-OR gates and 2-input AND gates. The total number of 2-input gates are proportional to the number of 1’s in the PCM. In order to represent every PCM Column in the SBEL block we first need to identify which of the following cases is applicable:

**Case 1:** Only 2-out-of-\( k \) (where \( m \) equals 2) code is used in the PCM. This is the simplest case where a single AND gate can individually represent any PCM column.

**Case 2:** If \( m = 2 \) and 3, then both types of column will need two 2-input AND gate. For \( m = 2 \), two inputs to the AND gate correspond to the 1’s from the first \( k \) bits of PCM column and the remaining input corresponds to the most significant residue bit. For \( m = 3 \), all three inputs to the AND gate correspond to the 1’s in the first \( k \) bits of the PCM column.

**Case 3:** If \( m \) equals 2 and 3 or 4, then 2 and 2 and 3 2-input AND gates are needed to represent individual PCM columns, respectively. For \( m = 2 \) and 3, see Case 2. For \( m = 4 \), all four inputs to the 2-input AND gate correspond to the 1’s in the first \( k \) bits of the PCM column.

H. Single Bit Error Corrector (SBEC)

Using the SBE output from the EI block, the (SBEC) block gets enabled only if either SBE is 1. In the other cases, the information bits are transmitted without correction. The inputs to the SBEC block include all information bits, output from the SBEL block along with the control output (SBE) from the EI block. The functionality of the SBEC block and SBEL block are identical to that used in [1]. In the presence of a SBE the SBEC block is enabled to correct the bit that is identified as erroneous by the SBEL block.

The method of obtaining the syndrome bits used was similar to Hsiao code and likewise the encoder can also be obtained from the first part of the decoder without using check bits as inputs. Additionally, the decoder also needs to compute the residue bits which are not required in the Hsiao encoder.

The proposed decoder significantly outperforms the decoder for Hsiao code for 64 or higher information bits in terms of 2-input gate count. In the following section, detailed analysis of the proposed code/decoder is presented.

### III. DISCUSSION OF RESULTS

The total number of 2-input gates used for decoding is significantly less in the proposed code than in Hsiao code. Table IV compares the Hsiao decoder with the decoder for the proposed; only 2-input gates and inverters are used to implement the decoder.

In Table IV, the negative percentages indicate the improvements of the proposed code over Hsiao code. For information bits 64 or high there is a significant difference in the gate usage; this can be primarily attributed to the design of the SBEL block. In order to locate an erroneous bit, every bit position is represented by a small network of 2-input AND gates based on their respective PCM column. In a Hsiao decoder, with \( n = 32 \), the PCM only uses 3-out-of-\( k \) code and therefore every column of the PCM can be represented by only two 2-input AND gates. In contrast, when \( n = 64 \), the PCM uses 3-out-of-\( k \) code as well as 5-out-of-\( k \) code, this requires \( (k-1) \) 2-input AND gates per PCM column, and in this case seven 2-input AND gates are needed since \( k = 8 \). If a bit error corresponds to a column with a 4-out-of-\( m \) code, then bit locations where \( m \) equals 2 or 3 will never be unintentionally corrected. This is because both of these cases incorporate the use of residue bits which unlike in Hsiao code eliminates the possibility of a bit being corrected erroneously. Hsiao decoder as mentioned previously can handle this by incorporating all the bits in a PCM column to identify SBE locations, at the expense of higher gate usage.

<table>
<thead>
<tr>
<th>( n )</th>
<th>( k )</th>
<th>( r )</th>
<th>HC</th>
<th>PC</th>
<th>Diff</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>8</td>
<td>2</td>
<td>109</td>
<td>151</td>
<td>-39</td>
</tr>
<tr>
<td>32</td>
<td>9</td>
<td>2</td>
<td>207</td>
<td>251</td>
<td>-42</td>
</tr>
<tr>
<td>64</td>
<td>10</td>
<td>2</td>
<td>737</td>
<td>450</td>
<td>-39</td>
</tr>
<tr>
<td>128</td>
<td>11</td>
<td>2</td>
<td>1643</td>
<td>946</td>
<td>-42</td>
</tr>
<tr>
<td>256</td>
<td>12</td>
<td>2</td>
<td>3621</td>
<td>2003</td>
<td>-45</td>
</tr>
</tbody>
</table>

In Table IV, the gate outputs are not shared to eliminate the risk of a multiple error resulting from a single stuck at fault. In the decoding circuit proposed in [1], the check bits are also corrected. Correcting any bit is simple once it is identified.
to be erroneous. The decoder for Hsiao code uses 3-input AND gates to identify the erroneous check bits when only 3-out-of-k code is used. This is not possible if all 3-out-of-m code words are used by the PCM; in other words a \((k - 1)\)-input AND gate is required to identify the check bits as well as information bits if check bit correction is required. Memory systems do not use check bits during computation, thus we have intentionally excluded the identification and correction of check bits in the decoder design.

IV. CONCLUSION

The main feature of the code in Ref.[4] is the reduced number of 1’s in the PCM. This results in an efficient encoding and decoding circuits for 64, 128, and 256 information bits. In addition the decoding of a syndrome pattern to identify the presence of a double bit error is considerably simplified. When the last two bits of a syndrome pattern are 11 a double bit error is immediately identified, no further decoding is necessary. When the last two bits are 00, 01 or 10, the decoding circuitry can locate and correct an erroneous bit or indicate the presence of a double/multi-bit error.

REFERENCES