3.5-bit Stage of the CMOS Pipeline ADC

Gao Wei, Xu Minglu, Xu Yan, Zhang Xiaotong, and Wang Xinghua

Abstract—A 3.5-bit stage of the CMOS pipelined ADC is proposed. In this report, the main part of 3.5-bit stage ADC is introduced. How the MDAC, comparator and encoder worked and designed are shown in details. Besides, an OTA which is used in fully differential pipelined ADC was described. Using gain-boost architecture with differential amplifier, this OTA achieve high-gain and high-speed. This design was using CMOS 0.18um process and simulation in Cadence. The result of the simulation shows that the OTA has a gain up to 80dB, the unity gain bandwidth of about 1.138GHz with 2pF load.

Keywords—pipelined ADC; MDAC; operational amplifier.

I. INTRODUCTION

HIGH performance Analog-to-Digital converters (ADCs) are critical parts in modern communication and signal processing systems. They are the interface between the analog and digital signal processing. With the development of modern communication, the trend of SOC pushes to integrate many separated module to one chip, achieve better performance and reduce the cost. In traditional communication receiver systems, there are 4 parts: RF modules, IF conversion, ADC and digital processing. If the ADC can directly deal with the intermediate frequency signal and its process is the same as digital part, the integrated chip will decrease the cost and save the area of the communication system.

This paper presents a stage 3.5-bit pipelined ADC. The article has 6 parts. After this introduction, we will give the introduction of the architecture of whole pipelined ADC system. In the third part, we will introduce the amplifier and other circuit used in design. The fifth part presents the simulation results to justify the conclusion. At last, it is on conclusions and discusses the applications.

II. THE ARCHITECTURE OF PIPELINE ADC

Following the sampling and hold amplifier, the pipelined stages have same modules including sub-ADC, MDAC and S/H [1], While, we only present only the first stage. According to the stages, the 3.5-bit codes are calculated following the order, that the front bit in the stage(i-1) is added to the last bit in the stage(i) and the carry is added to the front bit in the stage(i). The architecture of each stage and the structure of the whole pipeline system is indicated in Fig.1.

Gao Wei, Xu Minglu, Zhang Xiaotong and Wang Xinghua are with the School of Information and Electronics, Beijing Institute of Technology, Beijing, CO 100081 China (The corresponding author's e-mail: wxinghuad@ 126.com).
Xu Yan is with China Wuzhou Engineering Corporation LTD., China
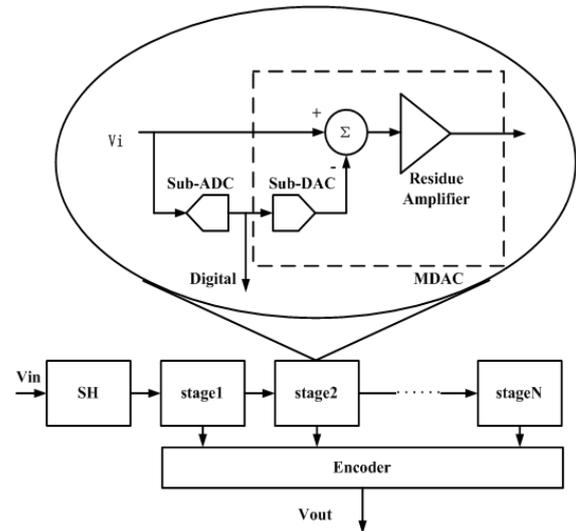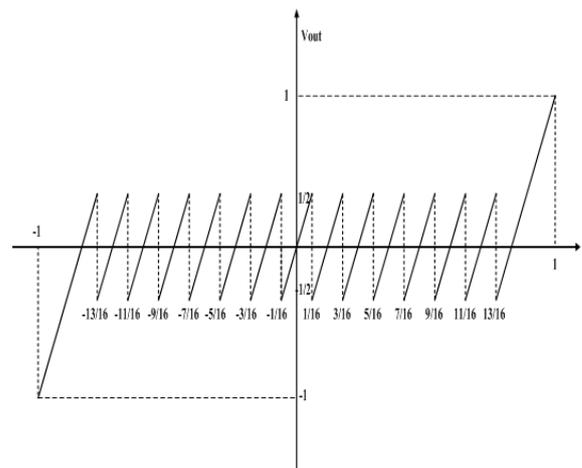
Fig. 1 General pipelined ADC architecture

Fig. 2 The transfer function of 3.5-bit stage

III. ARCHITECTURE OF PIPELINE STAGE

In this section the MDAC and sub-ADC module will shown, and some relation circuit such as encoder and comparator will also be introduced.

A. MDAC circuit

Within a pipelined stage, the functions of sample-and-hold, subtraction, DAC, and gain are commonly combined into a single switched capacitor circuit, referred to as a Multiplying Digital-to-Analog Converter (MDAC) [2]. The MDAC and the sub-AD C make up each pipelined stage in a pipe lined ADC. Instead of using a large number of reference voltage, the circuit achieve multiplication operation by applying numerous identical reference voltage which will simpler the schematic and layout.

World Academy of Science, Engineering and Technology
International Journal of Electronics and Communication Engineering
Vol:6, No:7, 2012

The architecture is showed in Fig. 3.
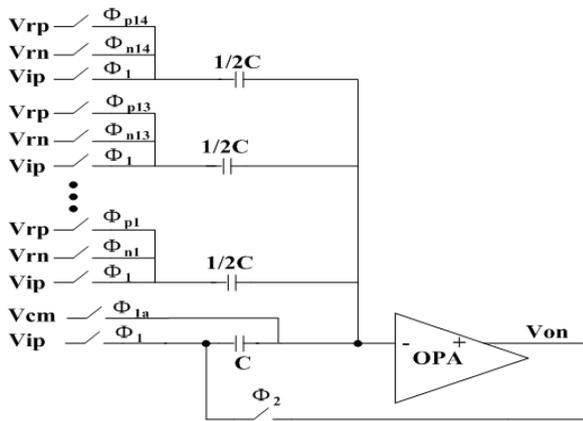

Fig. 3 Stage 3.5 bit MDAC circuit

During Φ1a the input is bottom plate sampled on capacitors. Bottom plate sampling significantly reduces the signal dependent charge injection on the sampling capacitors.

According to the theory of charge conservation, here is the output result,

$$V_{out} = 8 \cdot V_{in} - \left[\frac{\sum_{1}^{k} \frac{1}{2}C}{\sum_{1}^{2^{14}} \frac{1}{2}C} vrefp - \frac{\sum_{k+1}^{k} \frac{1}{2}C}{\sum_{1}^{2^{14}} \frac{1}{2}C} vrefn \right] \quad (1)$$

B. The sub-ADC

The sub-ADC circuit is used to convert the analog output of amplifier to digital code, the main part is constituted by dynamic comparator [3]. Combining the redundancy correction, the sub-ADC with bi effective number of bit consist of 2bi+1 resistors, 2bi+1-1 comparators. Here each 3.5-bit stage contains 14 comparators which present the binary code for the result of comparing the input signal and the references. Here is the schematic of comparator shown in Fig. 4.
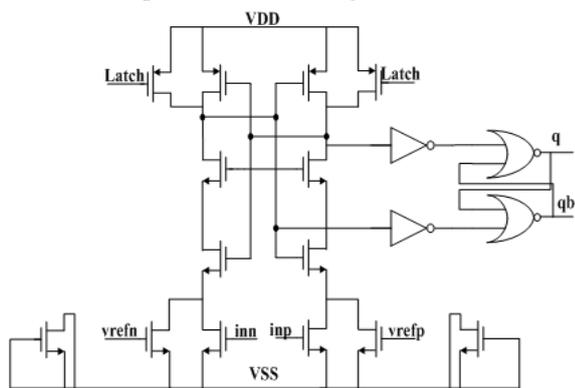

Fig. 4 The comparator circuit

C. The encoder

We suppose F<14>,F<13> ... F<1> as the expression of the output of the comparator. We can figure that: (Φp14,Φp13 ... Φp2, Φp1) = (F<14>, F<13> ... F<1>)
While Φn is the contrary output of Φp. So we can use the and

logic between the output of the comparator and the clock to achieve signals which control directly the switch in MDAC.

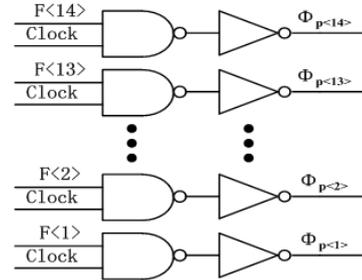Fig. 5 The encoder circuit

D. The architecture of operational amplifier

Based on the simulation of behavior model and estimate formulas [4], the requirements of amplifier for sampling-hold circuit are shown below.

Gain>80dB,GBW>500MHz ,SR>300V/us

Considering the range of common voltage and the swing of output [5], a kind of proposed fold-cascade amplifier is established, aiming at the specifications of this project. The architecture is shown below in Fig. 6.

In order to improve the driving ability, we use the structure in Fig.7, using cascade stage and common-drain stage to connect the amplifier, which will broaden the bandwidth while the dominant will not be influenced. But the common-mode level of the input has a necessary to be greater than 1.5v as a tradeoff to achieve the benefits above.

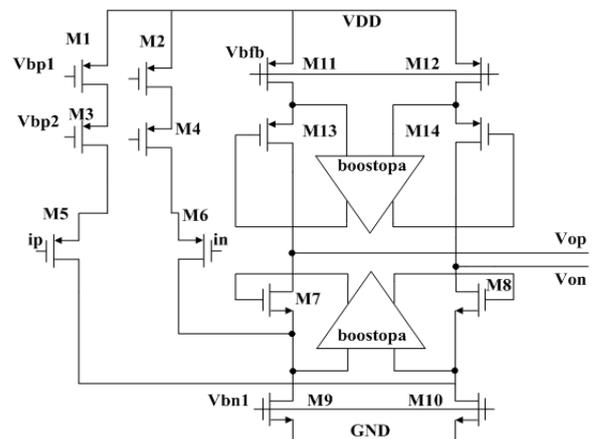And the structure of common-mode feedback used in the amplifier is indicated in Fig.8 [6].
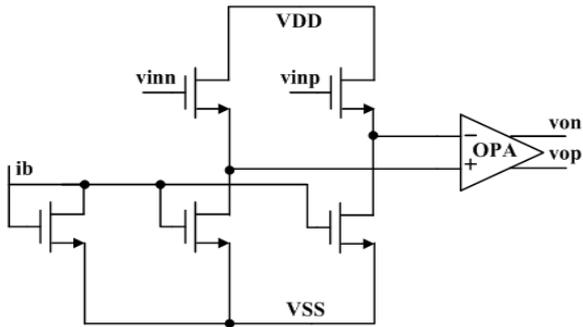

Fig. 6 The main form of the amplifier

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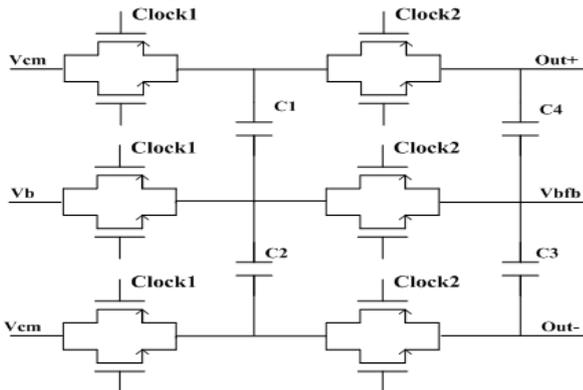Vol:6, No:7, 2012

Fig. 7 The structure of the OTA

Fig. 8 Common-mode feedback with switched-capacitor

IV. MEASUREMENT

The whole amplifier was design under TSMC 0.18 CMOS mix-signal process, and simulate using Specture under Cadence. Supply voltage is 1.8V, load capacitor is 2pF.

AC simulation result shows that DC-gain is 80.22 dB, unity gain bandwidth is 1.138GHz, Phase Margin is 68°, and slew rate is 303v /us. AC simulation result was shown in Fig. 9.
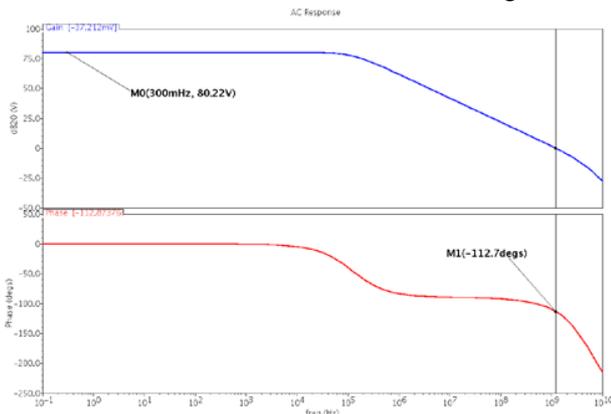

Fig. 9 AC response

The ADC has been fabricated in TSMC 0.18um one-poly six-metal CMOS process in 1.8V supply.

This project test is under the condition that the sampling frequency is 50MHz and the input is a slope signal with very slow change. The schematic of the whole stage 3.5-bit is shown in Fig.10 and the transience response result is shown in Fig.11.
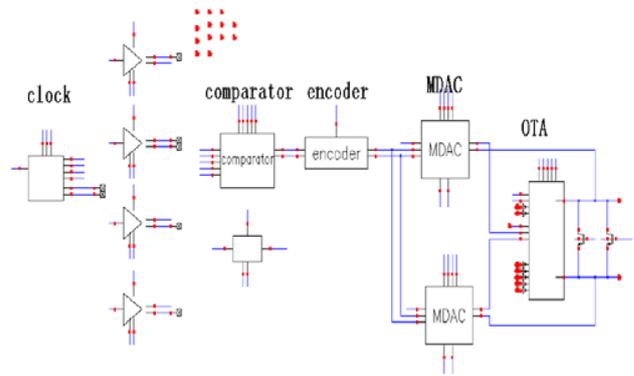
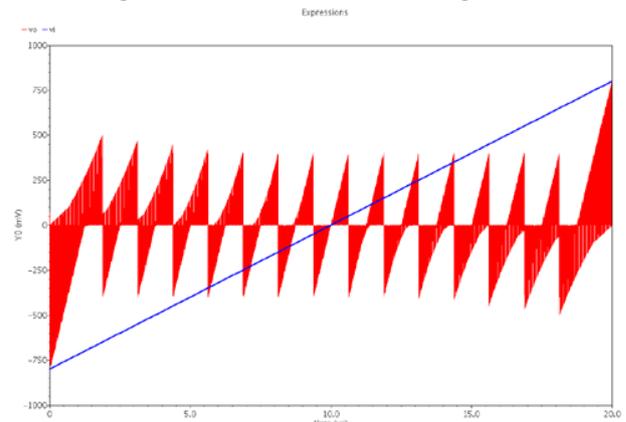

Fig. 10 The schematic of the whole stage 3.5-bit

Fig. 11 The transience response

The simulation result is identical with the transfer function. The circuit has achieved an accurate symmetry.

V. CONCLUSION

In this paper, a 3.5-bit stage of the CMOS pipelined ADC is described. Multi-bit MDAC, comparator and encoder circuit are introduced. In addition, instead of using single-ended amplifier, a fully differential amplifier is used in this paper. Besides, a CMFB circuit is used to reduce the jitter of the common-mode voltage. The result of schematic simulation is shown below: gain up to 80dB, unity gain bandwidth of about 1.138GHz for a 2pF load. Generally speaking, according to the performance of the stage 3.5-bit ADC, it can be widely used in multi-bit pipeline ADC system.

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