Symbolic Analysis of Input Impedance of CMOS Floating Active Inductors with Application in Fully Differential Bandpass Amplifier

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Abstract—This paper proposes a study of input impedance of 2 types of CMOS active inductors. It derives 2 input impedance formulas. The first formula is the input impedance of the grounded active inductor. The second formula is the input impedance of the floating active inductor. After that, these formulas can be used to simulate magnitude and phase response of input impedance as a function of current consumption with MATLAB. Common mode rejection ratio (CMRR) of the fully differential bandpass amplifier is derived based on superposition principle. CMRR as a function of input frequency is plotted as a function of current consumption.

Keywords—Grounded active inductor, floating active inductor, Fully differential bandpass amplifier.

I. INTRODUCTION

ACTIVE inductor implemented by CMOS technology was proposed since 1996 [1]. Usually, its inductance value is a function of current consumption and load capacitance. The more current consumption, the lower the inductance value. After that, there is considerable interest in quality factor (Q) enhancing technique of a grounded active inductor which was proposed since 2000 [2], because of low Q value and large silicon area of spiral inductor. By utilizing higher gain in the amplifier stage of the gyrator loop, the quality factor of a grounded active inductor can be improved to 12,000.

Another 2 papers on improving quality factor of a grounded active inductor was proposed in [3], [4]. The first circuit was based on the amplifier stage of the NMOS cascade transconductor cascade with feedback stage common source transistor. It has an additional feedback resistor between the output of amplifier stage of cascade transconductor and input of feedback stage of common source transistor. This circuit consumed less than 8 mW at 5.7nH at 1.55 GHz and it has Q of 70. The second circuit was based on amplifier stage of PMOS common source transconductor with feedback stage of PMOS common source transistor. It has an additional feedback resistor between the output of amplifier stage of PMOS common source transconductor and input of feedback stage of PMOS common source transistor. It also has additional capacitance at the output node of amplifier stage of PMOS common source transistor. The complete schematic is shown in Fig. 1.

Floating active inductor implemented in CMOS technology was first proposed since 2000 [5]. They designed differential oscillator at 1.2 GHz by consuming current approximately 220 microamperes. Another floating active inductor implemented in CMOS technology was proposed since 2006 [6]. They designed VCO with wide tuning range (143%) with 6-28 mW of power consumption at 0.5-3 GHz tuning range.

This paper organized as follows. Section II describes the first proposed circuit topology and derives the formula of the input impedance of the proposed circuit and its simulation results. Section III describes the second proposed circuit topology and derives the formula of the input impedance of the proposed circuit and its simulation results. The conclusion is given in Section IV.

II. THE PROPOSED GROUNDED ACTIVE INDUCTOR

The first proposed circuit is grounded active inductor based on amplifier stage of PMOS common source transconductor with feedback stage of PMOS common source transistor. It has an additional feedback resistor between the output of amplifier stage of PMOS common source transconductor and input of feedback stage of PMOS common source transistor. It also has additional capacitance at the output node of amplifier stage of PMOS common source transistor. The complete schematic is shown in Fig. 1.

Fig. 1 proposed grounded active inductor (a) transistor level (b) small signal equivalent of 1a

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The input impedance of Fig. 1 is derived as follows:

\[ z_{in} = \frac{s^2 c_2 + s c_1 + c_0}{s^4 f_4 + s^3 f_3 + s^2 f_2 + s f_1 + f_0} \]

\[ f_4 = a_2 c_2 - d_2 b_2 \]

\[ f_3 = (a_3 c_1 + c_2 a_1) - (d_3 b_1 + b_2 d_1) \]

\[ f_2 = (a_4 c_0 + c_2 a_0 + a_1 c_1) - (d_2 b_2 + b_2 d_0 + d_2 b_1) \]

\[ f_1 = (a_4 c_0 + c_0 a_0) - (d_1 b_0 + b_0 d_0) \]

\[ f_0 = a_0 c_0 - d_0 b_0 \]

\[ a_2 = (C_{p1} R_F) C_{p2} \]

\[ a_1 = \left( \frac{C_{g2} + C_{p1} + C_{g1} + C_{g2} + C_{g3}}{C_{l2}} + C_{p1} R_F \right) g_{m2} - g_{m1} R_F C_{g2} \]

\[ a_0 = -g_{m2} R_F \]

\[ b_1 = C_{g2} \left( 1 + \left( g_{m1} R_F + g_{m1} + g_{m2} R_F + g_{m2} + g_{m2} + g_{m2} \right) R_F \right) \]

\[ b_2 = C_{g2} \left( g_{m3} + g_{m2} + g_{m2} + g_{m2} + g_{m2} R_F \right) g_{m2} \]

\[ b_3 = \left( 1 + \left( g_{m1} R_F + g_{m1} + g_{m2} R_F + g_{m2} + g_{m2} \right) R_F \right) g_{m2} \]

\[ c_2 = \left( C_{g2} R_F + C_{g1} + C_1 \right) R_F C_{g2} \]

\[ c_1 = \left( C_{g2} R_F + C_{g1} + C_1 \right) \]

\[ c_0 = -g_{m1} R_F \]

\[ d_1 = (C_{p1} R_F) \]

\[ d_2 = (C_{p1} R_F) \]

\[ d_3 = (C_{p1} R_F) \]

\[ d_4 = \left( 1 + \left( g_{m1} R_F + g_{m1} + g_{m2} R_F + g_{m2} + g_{m2} \right) R_F \right) R_F \]

\[ d_5 = \left( g_{m2} R_F + g_{m2} + g_{m2} + g_{m2} + g_{m2} \right) R_F \]

\[ d_6 = \left( g_{m2} R_F + g_{m2} + g_{m2} + g_{m2} + g_{m2} \right) R_F \]

All coefficients in (1)-(3) are a function of parasitic capacitances, transconductances and drain to source conductances of the transistors and feedback resistor. Subscripts of the parameters indicate the name of the transistors.

The parameters used in the simulation with MATLAB are as follows. IdP1=IdN1=IdP2=IdN2=20uA, Rf=1kohm. The level1 0.5um CMOS process parameters which appeared in [8] are listed following lambda=0.1, lambda=0.2, VtoN=0.7, VtoP=-0.8, VON=460, VOP=115, Tox=9.5e-9.

Typical magnitude and phase response of grounded active inductor without drain to source conductance in Fig. 1 is shown in Fig. 2. It can be seen that phase response is not 90 or minus 270 degrees at all input frequencies. Thus, it can be seen that we use drain current only 20uA because it is the minimum current which aspect ratio of Mp1 can be designed to be larger than 1. And if we increased capacitive load from 0.5pF to 5pF, the resonance frequency of the input impedance of this circuit can be decreased from 330 MHz, 238MHz, 168MHz and 106 MHz, respectively.
Phase response can be seen from Fig. 2 as follows, for capacitive load of 0.5pF, phase response reaches minus 270 degrees. For capacitive load of 1pF, phase response could not reach minus 270 degrees. For capacitive load of 2pF, phase response could not reach minus 270 degrees. For capacitive load of 5pF, phase response could not reach minus 270 degrees. It can be concluded from this graph that at current of 20uA, input impedance of the circuit behaves like inductance as we increase the capacitive load. After input frequencies pass resonance frequency its impedance can become more capacitive.

The design parameters of circuit in Fig. 1 (b) which drain sourced conductances are not included which are listed as following.

- $R_f =$ feedback resistor = 1kohm
- $C_{gsp1} =$ gate to source capacitance of a transistor $M_{p1} = 1.97 \times 10^{-10}$ Farad
- $C_{gsp2} =$ gate to source capacitance of transistor $M_{p2} = 1.43 \times 10^{-10}$ Farad
- $C_{gsn1} =$ gate to source capacitance of transistor $M_{n1} = 2.28 \times 10^{-10}$ Farad
- $C_{gdp1} =$ gate to drain capacitance of transistor $M_{p1} = 5.37 \times 10^{-10}$ Farad
- $C_{gdp2} =$ gate to drain capacitance of transistor $M_{p2} = 3.91 \times 10^{-10}$ Farad
- Aspect ratio of $M_{n1} = 3.80$
- Aspect ratio of $M_{p1} = 3.29$
- Aspect ratio of $M_{p2} = 23.95$

Gate voltage of $M_{p1} = 2.5$ Volt, Gate voltage of $M_{p2} = 4$ Volt
The gate voltage of $M_{n1} = 5$ Volt, Supply voltage = 5 Volt
$V_{sbp1} =$ source bulk voltage of $M_{p1} = -1$ Volt
$V_{sbp2} =$ source bulk voltage of $M_{p2} = 0$ Volt
$V_{sbn1} =$ source bulk voltage of $M_{n1} = 4$ Volt

III. THE PROPOSED FLOATING ACTIVE INDUCTOR

The second circuit is floating active inductor based on 2 stages of the transconductor cascade with 2 stages of transconductor. The 2 stage transconductor composed of common gate transconductor as the first stage and common drain transconductor as the second stage. The complete schematic is shown in Fig. 4.
Fig. 4 Proposed floating inductors (FAI) (a) PMOS cross coupled oscillator FAI (b) small signal equivalent circuit of FAI

Fig. 5 Proposed floating active inductor (a) fully differential bandpass amplifier (b) small signal equivalent circuit of a fully differential bandpass amplifier

The input impedance of a floating active inductor in Fig. 4 (b) can be derived as follows equations.

\[ z_{in} = \frac{V_{in}}{I_{in}} = \frac{2\left( s^4 f_5 + s^3 f_4 + s^2 f_3 + s f_2 + f_1 \right)}{s^4 k_5 + s^3 k_4 + s^2 k_3 + s k_2 + k_1} \]

\[ k_5 = h_i \left( C_{pr3} + C_{pr1} \right) + i_i \left( C_{pr3} + C_{pr1} \right) \]

\[ k_5 = g_{d tot} s - h_i \left( C_{pr3} + C_{pr1} \right) \]

\[ -i_i \left( g_{m3} + g_{m1} \right) - i_i \left( C_{pr3} + C_{pr1} \right) \]

\[ k_4 = g_{d tot} s = h_i \left( C_{pr1} + C_{pr3} \right) \]

\[ -i_i \left( g_{m3} + g_{m1} \right) - i_i \left( C_{pr1} + C_{pr3} \right) \]

\[ k_3 = g_{d tot} s = -h_i \left( C_{pr1} + C_{pr3} \right) \]

\[ -i_i \left( g_{m3} + g_{m1} \right) - i_i \left( C_{pr1} + C_{pr3} \right) \]

\[ k_2 = g_{d tot} s = -h_i \left( C_{pr1} + C_{pr3} \right) \]

\[ -i_i \left( g_{m3} + g_{m1} \right) - i_i \left( C_{pr1} + C_{pr3} \right) \]

\[ k_1 = g_{d tot} s = -i_i \left( C_{pr1} + C_{pr3} \right) \]

\[ -i_i \left( g_{m3} + g_{m1} \right) - i_i \left( C_{pr1} + C_{pr3} \right) \]

\[ k_0 = g_{d tot} s = -i_i \left( C_{pr1} + C_{pr3} \right) \]

\[ f_5 = h_d d_5 f_5 = (h_d d_5 + h_d d_5 + h_d d_5) f_5 = (h_d d_5 + h_d d_5 + h_d d_5) \]

\[ f_4 = (h_d d_4 + h_d d_4 + h_d d_4) f_4 = (h_d d_4 + h_d d_4 + h_d d_4) \]

\[ g_3 = a_d d_3 g_3 = (a_d d_3 + a_d d_3 + a_d d_3) g_3 = (a_d d_3 + a_d d_3) \]

\[ g_2 = (a_d d_2 + a_d d_2 + a_d d_2) g_2 = (a_d d_2 + a_d d_2) \]

\[ h_2 = h_m d_2 h_2 = (h_m d_2 + h_m d_2 + h_m d_2) \]

\[ h_1 = (h_m d_1 + h_m d_1 + h_m d_1) h_1 = (h_m d_1 + h_m d_1 + h_m d_1) \]

\[ i_3 = c_3 h_3 i_3 = (c_3 h_3 + c_3 h_3) i_3 = (c_3 h_3 + c_3 h_3) \]

\[ i_2 = (c_2 h_2 + c_2 h_3) i_2 = (c_2 h_2 + c_2 h_3) i_2 = (c_2 h_2 + c_2 h_3) \]

\[ i_1 = (c_1 h_1 + c_1 h_2) i_1 = (c_1 h_1 + c_1 h_2) i_1 = (c_1 h_1 + c_1 h_2) \]
After that, it falls dramatically to minus 90.6 degrees at 11.8 GHz.

For sys, which is shown in blue solid line, the current is designed to be 10 microamperes. The magnitude response arises from minus 126 dB at 1 MHz until it reaches resonance frequency 10.2 GHz at 67.6 dB. The phase response for this current consumption starts from 0 degree. It rises slowly at 100 MHz until it reaches 73.1 degrees at 7.65 GHz. After that, it falls tremendously to minus 90.6 degrees at 12.8 GHz.

For sys2, which is shown in red dotted line, the current is designed to be 20 microamperes. The magnitude response arises from minus 114 dB at 1 MHz until it reaches resonance frequency 9.23 GHz at 60.9 dB. The phase response for this current consumption starts from 0 degree. It rises slowly at 100 MHz until it reaches 71.5 degrees at 7.74 GHz. After that, it falls dramatically to minus 90.5 degrees at 11.5 GHz.

For sys3, which is shown in cyan dashed line, the current is designed to be 30 microamperes. The magnitude response arises from minus 107 dB at 1 MHz until it reaches resonance frequency 8.93 GHz at 61.7 dB. The phase response for this current consumption starts from 0 degree. It rises slowly at 100 MHz until it reaches 69.7 degrees at 7.24 GHz. After that, it falls sharply to minus 90.5 degrees at 10.4 GHz.

All coefficients in (4)-(7) are a function of parasitic capacitances, transconductances and drain to source conductances of the transistors and feedback resistor. Subscript of the parameters indicates the name of the transistors.

The parameters used in the simulation with MATLAB are as follows. ldP1=ldP1=ldP3=ldP4=1uA,10uA,20uA,30uA.

ldn5=ldn6=1uA,10uA,20uA,30uA, respectively. The level1 0.5um CMOS process parameters which appeared in [8] are as follows lambdaN=0.1, lambdaP=0.1, VtoN=0.7, VtoP=0.8, UON=460, UOP=115, Tox=9.5e-9. For graph in Fig. 6, we used a minimum length to be 1 micron.

Typical magnitude and phase response of the floating active inductor is shown in Fig. 6. For sys4, which is shown in black dashed dotted line, the current is designed to be 1 microampere. The magnitude response arises from minus 166 dB at 1 MHz until it reaches resonance frequency 9.13 GHz at 85.2 dB. The phase response for this current consumption starts from 0 degree. It rises slowly at 100 MHz until it reaches 69.5 degrees at 7.4 GHz.
\[ I_1 = (C_{C1} + C_1) f_1 + k_1 \]
\[ I_2 = (C_{C2} + C_2) f_2 + \left( \frac{1}{R_1} \right) f_1 + k_2 \]
\[ I_3 = (C_{C3} + C_3) f_3 + \left( \frac{1}{R_2} \right) f_1 + k_3 \]
\[ I_4 = (C_{C4} + C_4) f_4 + \left( \frac{1}{R_3} \right) f_1 + k_4 \]
\[ I_5 = (C_{C5} + C_5) f_5 + \left( \frac{1}{R_4} \right) f_1 + k_5 \]
\[ I_6 = (C_{C6} + C_6) f_6 + \left( \frac{1}{R_5} \right) f_1 + k_6 \]
\[ I_7 = \left( \frac{1}{R_6} \right) f_1 + k_7 \]

\[ m_x = 2C_{f,1} f_1 + k_1, m_y = 2C_{f,1} f_1 + \frac{2f_1}{R_1} + k_1 \]
\[ m_x = 2C_{f,2} f_1 + \frac{2f_1}{R_2} + k_1, m_y = 2C_{f,2} f_1 + \frac{2f_1}{R_2} + k_1 \]
\[ m_x = 2C_{f,3} f_1 + \frac{2f_1}{R_3} + k_1, m_y = 2C_{f,3} f_1 + \frac{2f_1}{R_3} + k_1 \]
\[ n_x = 2f_2 g_{d,2} + 2C_{g,p} f_3 + m_3 \]
\[ n_y = 2f_2 g_{d,3} + 2C_{g,p} f_3 + m_4 \]
\[ n_z = 2f_2 g_{d,4} + 2C_{g,p} f_3 + m_5 \]
\[ n_l = 2f_3 g_{d,5} + 2C_{g,p} f_3 + m_6 \]
\[ n_x = 2g_{d,1} f_6 + m_0 \]

\[ g_y = g_{d,2} + g_{d,3} + g_{d,4} + g_{d,5} - g_{d,6} - g_{d,7} - g_{d,8} \]

\[ C_j = \left( C_{g,p} + C_{g,r} + C_{g,1} \right) \]

\[ a_1 = n_1 C_1, a_2 = n_2 C_1 + n_2 g_y, a_3 = n_3 C_1 + n_3 g_x, a_4 = n_4 C_1 + n_4 g_{y,1} - 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_1 \]
\[ a_5 = n_5 C_1 + n_5 g_{y,2} - 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_1 \]
\[ a_6 = n_6 C_1 + n_6 g_y - 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_1 \]
\[ a_7 = n_7 C_1 + n_7 g_y - 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_1 \]
\[ a_8 = n_8 C_1 + n_8 g_y - 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_1 \]
\[ a_9 = n_9 C_1 + n_9 g_y - 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_1 \]
\[ a_{10} = n_{10} C_1 + n_{10} g_y - 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_1 \]

\[ p_1 = m_1 C_1, p_2 = m_2 C_1 + m_2 g_x, p_3 = m_3 C_1 + m_3 g_y + 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_5 \]
\[ p_4 = m_4 C_1 + m_4 g_{y,1} + 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_6 \]
\[ p_5 = m_5 C_1 + m_5 g_{y,2} + 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_7 \]
\[ p_6 = m_6 C_1 + m_6 g_y + 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_8 \]
\[ p_7 = m_7 C_1 + m_7 g_y + 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_9 \]
\[ p_8 = m_8 C_1 + m_8 g_y + 2g_{d,8} \left( g_{d,8} - g_{d,9} \right) f_10 \]
\[
\begin{align*}
V_o &= -(2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, 2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, 2p_f, 2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, 2p_f, 2p_f, 2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, s_f) \\
V_{\text{in}} &= (2p_f + 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, 2p_f, s_f)
\end{align*}
\]
Fig. 7 Typical Magnitude and phase response of common mode rejection ratio (CMRR) of fully differential bandpass amplifier as a function of drain current $R_L = 10\Omega$

Fig. 8 Typical Magnitude and phase response of differential mode gain (Adm) of fully differential bandpass amplifier as a function of drain current $R_L = 10\Omega$
Fig. 9 Typical Magnitude and phase response of common mode gain (Acm) of fully differential bandpass amplifier as a function of drain current $R_L = 104\Omega$

**IV. CONCLUSION**

From a simulation with MATLAB, it can be concluded that center frequency and the voltage gain of a fully differential bandpass amplifier can be tuned by adjusting values of capacitive load, resistive load, $L_{CR}$ and minimum length of transistors in Fig. 4 (a). The higher is the current, the lower the center frequency. It can be seen from the graph of differential mode gain in Fig. 7 that differential mode gain can be designed to be 5 dB at center frequency of 1.16 GHz at current consumption of 8 mA. It can be seen that for current consumption of 4mA, $A_{dM}$ can be designed to be minus 3.86 dB at center frequency of 1.46 GHz. It can be concluded that this circuit consumed very high current if voltage gain is a stringent requirement.

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