Temperature Sensor IC Design for Intracranial Monitoring Device

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Abstract—A precision CMOS chopping amplifier is adopted in this work to improve a CMOS temperature sensor high sensitive enough for intracranial temperature monitoring. An amplified temperature sensitivity of $18.8 \pm 3.02 \, \text{mV/}^\circ\text{C}$ is attained over the temperature range from 20 °C to 80 °C from a given 10 samples of the same wafer. The analog frontend design outputs the temperature dependent and the temperature independent signals which can be directly interfaced to a 10 bit ADC to accomplish an accurate temperature instrumentation system.

Keywords—Chopping; analog frontend; CMOS temperature sensor; traumatic brain injury (TBI); intracranial temperature monitoring.

I. INTRODUCTION

Traumatic brain injury (TBI) is a severe damage to a brain by an external force, and it can cause the intracranial temperature to rise up to few degrees in Celsius over the body temperature [1]. However, it is still not clear whether the raised intracranial temperature is an adaptive response to the trauma or a harmful outcome to the brain tissue [2]. Therefore, in addition to monitoring the level of the brain pressure and the dissolved oxygen, it is a common practice in the hospital to equip with continuous intracranial temperature monitoring systems such that the physician can acquire the TBI patient’s brain temperature at any time. Failing in accessing the update and an accurate intracranial temperature can have an adverse effect in managing the patient health.

Temperature sensing applications are heavily employed in academic, commercial, industrial, and medical community. For high precision temperature sensor, the sensor choice is usually a platinum based resistance temperature detector (RTD). Many commercial RTDs can measure ambient temperature in a precision of less than 0.1 °C. Nonetheless, the material is very expensive, and it requires an external instrumentation system to be set up.

An alternative choice to a RTD is a parasitic vertical bipolar transistor in standard CMOS platform. The device is very well modeled in commercial foundries, so a lot of designers have been using this device for creating temperature sensing applications. Ideally speaking, it is more favorable and practical to develop a temperature sensor in CMOS technology as the sensor can be made more robust and intelligent by designing an application specific integrated circuit (ASIC) on the same substrate. We discussed elsewhere the specific requirements on the temperature sensors and the various system architectures to interface the sensor for intracranial applications [3].

In this work, we will illustrate the application of chopping stabilization to realize a high sensitive temperature sensor for intracranial temperature monitoring, which requires a 0.1 °C inaccuracy over 10 °C temperature sensing range. The goal of this work is to increase the temperature sensitivity of the sensor precisely for interfacing with a 10 bit A to D converter.

II. CONVENTIONAL CMOS TEMPERATURE SENSORS: PRINCIPLE AND PRACTICE

Shown in Fig. 1 is a reference design in a typical temperature sensor instrumentation system.

![Fig. 1 Temperature sensor instrumentation system](image)

Fig. 1 is made up of 3 cores: a $V_{BE}/AV_{BE}$ generator, a bandgap reference ($V_{BE}$) generator, and an A to D data converter. The bias current $I_b$ is defined in the $V_{BE}/AV_{BE}$ generator, which consists of the two parasitic vertical bipolar transistors $Q_1$ and $Q_2$ using the same value of current bias. Assuming that the offset voltage $V_{os}$ of the operational transistor (OTA) is negligible, the expression of $I_b$ can be approximated by (1).

$$I_b = \frac{V_{BE2} - V_{BE1}}{R_1}$$

Equation (1) holds true when the OTA is biased in high gain operation such that the non-inverting input and the inverting input are in virtual short. In other words, the base emitter voltage of $Q_2$ will be equal to the base emitter voltage of $Q_1$ plus the ohmic voltage drop across the resistor $R_1$.

Equation (1) is an approximation because the forward current gain $\beta$ of the bipolar transistors is assumed negligible, so the collector current of the bipolar transistors can be assumed to be equal to the bias current $I_b$. [Image 309x362 to 547x558]
Consequently, the base-emitter voltage of the bipolar transistor can be represented by (2).

\[ V_{BE} = V_T \ln \left( \frac{I_b}{I_s} \right) \]  

where \( V_T = (kT/q) \) is the thermal voltage and \( I_s \) is the saturation current of the bipolar transistors. It is known that the saturation current has a strong dependency to temperature, so the base emitter voltage is non-linear dependent to temperature. To a 1st order approximation, the temperature sensitivity of the base-emitter voltage is non-linear dependent to temperature. To a 1st order approximation, the temperature sensitivity of the PTAT voltage and the CTAT voltage can be expressed as (4):

\[ V_{BE} = V_{BE3} + \frac{R_2}{R_1} V_T \ln(n) \]  

With reference to the temperature instrumentation system as shown in Fig. 1, the base emitter voltage and the bandgap reference voltage are connected directly to the input channel and the reference channel of the ADC respectively. For a typical CMOS OTA with 1.8 Volt input range, the least significant bit (LSB) is 1.76 mV. For a temperature precision of 10°C, the intended application is restricted to 10°C. Lastly but not least, the inaccuracy of the base-emitter voltage or the bandgap voltage due to the process mismatch was well documented [4], [5]. To sum up, other than the offset due to the OTA, the temperature offset error is depended on the process spread of the saturation current of the vertical bipolar transistors, the limited value of the forward current gain of the bipolar transistors, the current mirror mismatch, and the mismatch of the passive resistors \( R_1 \) and \( R_2 \). All these mismatches should be minimized and trimmed such that the design can be applicable for the typical temperature measurement range. In the scope of this work, the intended application is restricted to 10°C, so the use of chopper stabilization technique, together with a digital trimming on the resistance, are suffice to achieve the inaccuracy of 0.1°C.

III. CMOS CHOPPER STABILIZED TEMPERATURE SENSOR INSTRUMENTATION SYSTEM

A. \( V_{BD}/AV_{BE} \) Generation based on chopper stabilization

The concept of chopper stabilization amplifier was well discussed and analyzed in [6], and it is briefly summarized here. Shown in Fig. 2 illustrates a chopper system where the input signal \( V_{in} \) is first up-converted to the chopping frequency \( f_{chop} \) before going to the amplifier A1. The amplifier has a DC offset \( V_{os} \). After amplification, the amplified signal \( A^*V_{in} \) will undergo demodulation such that the ac-amplified signal is moved back to the baseband. On the other hand, the amplified offset \( A^*V_{os} \) will be up-converted to the chopping frequency \( f_{chop} \). Therefore, the output of the chopping amplifier is a DC offset-free amplified baseband signal superimposed of an ac-amplified offset situated at the chopping frequency \( f_{chop} \). Nonetheless, the output of the chopping amplifier has to be low pass filtered so as to eliminate the ac modulated offset.
which highlights the $V_{BE}/\Delta V_{BE}$ generator only. The OTA is replaced by the chopping amplifier. In this way, 32 different values of resistance can be generated, and the equivalent base emitter voltage can be adjusted accordingly.

![Fig. 3 V$_{BE}$/$\Delta$V$_{BE}$ generation employing a chopping amplifier](image_url)

Shown in Fig. 3 is an improved version of the $V_{BE}/\Delta V_{BE}$ generator which employs chopper stabilization. The amplifier offset $V_{os}$ is modulated once; this offset will be amplified and modulated to the chopping frequency, but this frequency modulated offset will be eliminated by the low pass filter (LPF). On the other hand, the inputs of the amplifier (i.e., the base emitter voltage of the parasitic vertical pnp transistors $Q_1$ and $Q_2$) are modulated twice, so they will be amplified at ac under the closed loop configuration and demodulated down to DC. Consequently, the voltage bias to the PTAT current sources is offset free, which is the key to achieve an accurate bandgap voltage and the temperature sensing signal $V_{BE}$.

**B. V$_{BE}$ tuning**

To achieve the temperature output with an inaccuracy of ±0.1 °C, other sources of offset has to be compensated. For instance, the current mismatch on the PTAT current source, the resistor mismatch between $R_1$ and $R_2$, and the finite value of the forward current gain of the parasitic vertical pnp transistors all contributed to the mismatch on the temperature acquisition system. To ensure high precision, a one point calibration of the base emitter voltage of the pnp transistor $Q_3$ at room temperature is done via a digital trimming. The trimming can be done by trimming the emitter area, the PTAT current source, and the resistance. Under normal consideration of the design of the trimming network is to trade off the use of the chip area with the resolution of the trimming. In our design, resistance trimming is employed, and it is sketched in Fig. 4. Note that there are 32 switches connecting to 32 identical resistors in parallel. The control of the switches is done via a 5-to-32 decoder. The decoder generates only one active output high whereas all the other outputs are active low. There decoder outputs are connected to all the switches individually so that only one of the switches can be turned on.

![Fig. 4 V$_{BE}$ voltage trimming](image_url)

**C. V$_{BE}$ amplification**

To achieve the temperature output with an inaccuracy of ±0.1 °C, the resolution of the ADC should be 0.1 °C/LSB or lower. For a 10-bit ADC which does the AD conversion for a given bandgap reference voltage, the temperature signal $V_{BE}$ has to be amplified in order to achieve the required resolution. In the silicon implementation, the temperature sensitivity of the trimmed $V_{BE}$ signal is amplified by 10 times to achieve the required temperature resolution. The design is sketched in Fig. 5.

![Fig. 5 V$_{BE}$ amplification scheme](image_url)

Note in Fig. 5 that the $\alpha V_{BG}$ is a bandgap reference voltage with the scale factor $\alpha$. The expression of the signal $V_{TEMP}$ can be represented by (6).

$$V_{TEMP} = \alpha V_{BG} - V_{BE}\left(\frac{R_2}{R_1}\right)$$

Since the closed loop gain, which is equal to $\frac{R_2}{R_1}$ is not small, a chopper stabilized amplifier is a preferred choice for achieving the required closed loop gain in the presence of any DC offset of the amplifier.

**IV. SILICON MEASUREMENT RESULTS**

The analog front end CMOS chopper stabilized temperature sensor instrumentation system was realized in a 0.18um 1P6M CMOS process, and it is packaged in a DIP28 for evaluation purpose. The die photo is shown in Fig. 6.
The core circuit has a dimension of 0.3mm x 0.9mm. The chip consumes less than 200 µA current consumption under typical condition.

Fig. 6 Chip microphotograph

The experimental setup consists of a custom designed printed circuit board to interface the chip. The board provides test points to the bandgap voltage (VBG) and the amplified base emitter voltage signal (VTEMP). Besides, there is an on board crystal oscillator which provides a chopping frequency of 125 kHz. The board was placed inside an oven whose temperature can be adjusted through the GPIB interface. The output signals were captured by the external multimeters, which can send the data to a laptop through the same GPIB interface. Ten chips on the same wafer were evaluated, and the results are presented in the following.

Fig. 7 shows the measured bandgap reference voltage versus temperature. Although the intended temperature sensing range is specified to 10 °C, the chip can work well in the temperature range from 20 °C to 80 °C. In particular, the bandgap voltage mismatch is within 20 mV over the 10 chips. This amount of offset can be attributed to the offset associated with the output voltage buffer for probing the bandgap voltage. The temperature instability of this bandgap reference design is below 45 ppm.

Fig. 8 shows the variation of the measured temperature sensitivity over the 10 chips. The mean temperature sensitivity is found to be 18.8 mV/°C with a standard deviation of 0.24 mV/°C. Thus, the fabricated analog front-end design is able to achieve a temperature signal with a resolution of 0.1 °C/LSB for the 10-bit ADC. The temperature error due to the mismatched sensitivity is under 1.3%, which can be further reduced by the resistor trimming network.

Fig. 8 Variation of temperature sensitivity over the 10 samples

The performance summary of the chopper stabilized temperature sensor analog front-end is tabulated in TABLE I.

<table>
<thead>
<tr>
<th>Process</th>
<th>0.18μm 1P6M CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of samples</td>
<td>10</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>3.3 Volts</td>
</tr>
<tr>
<td>Current consumption</td>
<td>200 µA</td>
</tr>
<tr>
<td>Chopping frequency</td>
<td>125 kHz</td>
</tr>
<tr>
<td>Temperature range</td>
<td>20 °C to 80 °C</td>
</tr>
<tr>
<td>Bandgap temperature instability</td>
<td>&lt; 45 ppm</td>
</tr>
<tr>
<td>Temperature sensor sensitivity</td>
<td>18.8 mV/°C</td>
</tr>
</tbody>
</table>

TABLE II

V. CONCLUSION

A CMOS temperature sensor analog frontend utilizing chopper stabilization has been presented in this work. A high precision bandgap voltage is realized by the use of chopping to eliminate the DC offset, if any, from the amplifier used for the PTAT generation.

Further offsets due to the process mismatch are suppressed by a 5-bit resistor trimming network.
On the other hand, an amplified temperature sensitivity of the base-emitter voltage is achieved by amplifying the base-emitter voltage such that the amplified signal can accomplish a resolution of 0.1 °C/LSB for the given 10 bit ADC.

ACKNOWLEDGMENT

The work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research), Singapore, under the grant number: 102 148 0002.

REFERENCES


