A 1.5V, 100MS/s, 12-bit Current-Mode CMOS Sample-and-Hold Circuit

O. Hashemipour, and S. G. Nabavi

Abstract—A high-linearity and high-speed current-mode sample-and-hold circuit is designed and simulated using a 0.25μm CMOS technology. This circuit design is based on low voltage and it utilizes a fully differential circuit. Due to the use of only two switches the switch related noise has been reduced. Signal-dependent error is completely eliminated by a new zero voltage switching technique. The circuit has a linearity error equal to ±0.05μA, i.e. 12-bit accuracy with a ±160μA differential output - input signal frequency of 5MHz, and sampling frequency of 100MHz. Third harmonic is equal to –78dB.

Key words—Zero-voltage-technique, MOS-resistor, OTA, Feedback-resistor.

I. INTRODUCTION

Sample and hold (S/H) Circuits are important block in data converter systems, such as the front end of A/d Converters. Up to present time, considerable numbers of circuits were designed for S/H in voltage and current mode. Recently more focus is on current-mode circuits due to high speed and low voltage supply in comparison with voltage-mode (switched-capacitor) circuits.

Unfortunately, charge injection error is the main problem of S/H circuits resulting in accuracy reduction of these circuits and hence the creation of non-linearity distortion.

A number of circuits were designed in order to improve either high-speed or high-accuracy [1, 2, 3, 5]. For example, the circuit in [3] which is shown in Fig. 1, is a high accurate switched-current-memory-cell around 14-bit resolution using zero-voltage technique. In order to remove the signal-dependent-error a constant voltage is set at the sampling switch using a High-gain-opamp and a negative-feedback circuit. This design lacks the speed of operation due to gm considerations; however, it is one of the most accurate SI circuits.

In this work, with the aid of two simple OTA and two MOS-resistors a constant voltage on both sides of switches are generated during sample and hold mode resulting in complete removal of signal-dependent-error and the offset-error part is also canceled out by using the fully-differential outputs.

II. CIRCUIT OVERVIEW

The circuit block diagram is shown in Fig. 2. It constitutes a differential input stage and three simple OTAs, two Sampling switches and MOS-feedback-resistors. In sampling phase, after closing switches, differential input current between OTA-m in upper part and OTA-A, B is divided in K, and K’ ratio respectively. The current at the output nodes will be: I_{out} = I_{in} and I_{out}’ = –I_{in}. In holding phase the output currents will be equal to input currents. During both phases the two OTAs A and B will hold a constant voltage (V_G) at switches terminals. In order to eliminate the signal dependent error, active feed-back resistors are used for stabilization of V_G.

III. COMPLETE CIRCUIT DESIGN

Fig. 3 shows the designed S/H circuit. It consists of transistors M_{3-5}, M_{8, M_m and M_n} for differential input stage, transistors M_{1-2, M_6-7, and M_{9-10}} for OTA - M, transistors M_{11, M_{1c11, M_{13, M_{1c13, M_r}}}, and M_{1f2} for OTA-A, transistors M_{12, M_{1c12, M_{14, M_{1c14, M_h}}}, and M_{1f2} for OTA - B, transistors M_{S1 and M_{S2}} are sampling switches and finally M_{1c1} and M_{r2} are MOS-resistors. Common mode feed back circuit is used in order to stabilize the common mode voltage of the fully differential opamp. During sampling mode while
switches $M_{S1}$ and $M_{S2}$ are closed, part of the input differential signal, $\pm K I_{in}$ will be at the outputs of OTA-M and the other part, $\pm K' I_{in}$ after inversion will be at outputs of OTA-A and OTA-B:

$$I_{out} = K' I_{in} + K I_{in} = (K + K') I_{in} \quad (1)$$

$$I_{out} = -K' I_{in} - K I_{in} = -(K + K') I_{in} \quad (2)$$

For input and output currents to be equal:

$$K + K' = 1 \quad (3)$$

The dimensions of $m$ and $m_n$ are adjusted in order to satisfy (3). In this design the $K$ and $k'$ factors are equal to 2/3 and 1/3 respectively and

$$(W/L)_{m,n} = (W/L)_{f,1,2,3,4} = 2/3(W/L)_{1,2,3,4}$$

in order to keep the circuit fully balanced.

### A. Charge Injection Error Cancellation

Signal-dependent charge-injection arises when the voltage at a switch's sampling terminals varies with the signal level. To avoid signal-dependent-error, the voltage at the terminals of switch must remain at a constant level. In this work, due to fully balanced structure of the different stages during sampling period the voltage at $V_A = V_B = V_G$ is equal to the drain voltages of transistor $M_{C11}$ and $M_{C12}$. During holding period the above voltages must be kept constant. However, practically open loop gain of the OTAs are not high enough to achieve this, and hence a feedback-resistors network is utilizing using two transistors $M_{11}$ and $M_{12}$ in order to provide constant voltage in node A and B. This is due to the fact that in holding mode voltage at input nodes are equal to drain voltage of the transistors $M_{C11}, M_{C12}$ and voltage and bias voltage $V_G$, therefore, using large feedback-resistors from drain of $M_{C11}$ and $M_{C12}$ to nodes A and B, the voltage level of these nodes will be equal to $V_G$. This means nodes A and B are virtual ground and therefore during sampling and hold mode the terminal voltages of switches are constant and equal to $V_G$, thus error is independent of input signal.

### B. Speed of Circuit

Time-constant in basic SI circuits is equal to $\tau \approx (C g/m)$. In order for speed to be increased, $g/m$ must be increased, i.e. increase the bias-current. This of course will result in an increase in both noise and power dissipation. In this work, the speed improvement of the circuit is achieved by using high-speed OTAs and small memory capacitors $C_{g1}$ and $C_{g2}$. Moreover, diode connected loads are used instead of current sources in order to increase $g/m$, the time constant is now:

$$\tau \approx C g/m \left( g_{m3} + g_{m4} \right) \quad (4)$$

Diode connected loads will also result in a decrease in the input impedance of the circuit, from typical value of $1/g_m$ in basic SI to $1/(g_{m3} + g_{m4})$ in this work. Lower input impedance will results in a decrease in distortion.

### IV. Simulation Results

The proposed S/H circuit has been designed and simulated using Hspice and the 0.25μm CMOS technology and input-signal-frequency of 5MHz in full-scale mode. The full-scale value of the input current is ±80μA with a sampling frequency of 100MHz. Fig. 4 shows the differential sinusoidal current
Fig. 3 Complete sample and hold circuit

The biasing current is 300μa and the hold-capacitors $C_{g1}$ and $C_{g2}$ are 0.26pf. The supply voltage Vdd is 1.5V and the power-dissipation of the circuit is 2.5mW. The differential current output is ±160μa. Simulation results from a triangular input signal with 5MHz frequency and ±80μa range, measurements shown in Fig. 5 results in a linearity-error of about 0.05μa. This much error is equal to 12-Bit resolution for an S/H circuit.

Fig. 4 Differential output current

The total-harmonic-distortion is extracted using PSD output waveform and FFT-method as in [4]. Fig. 6 shows the PSD waveform which results in a 3rd harmonic of less than –78dB. The FFT simulation is performed by using sinusoidal-input signal frequency of 4.88MHz, and a sampling frequency of 100MHz. As shown in Fig. 7 simulation was performed for different input frequency range of 1.22 MHz to 8.544 MHz and the results shows a resolution of 12-Bit under all conditions. Table I shows a summary of the performance of the designed S/H circuit.

Fig. 5 Triangular output signal for linearity-error Measurement
Fig. 6 PSD waveform of sinusoidal response of S/H circuit

Fig. 7 THD% versus Input-frequency

The presented S/H circuit is suitable for SI systems requiring precise sample-and-hold circuit.

REFERENCES

TABLE I
SUMMARY OF SIMULATION RESULTS

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.25μm CMOS</th>
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<tbody>
<tr>
<td>Supply voltage</td>
<td>1.5V</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>2.5Mw</td>
</tr>
<tr>
<td>HD3 @ 100MHz-clock &amp; 4.88MHz input frequency</td>
<td>-78dB</td>
</tr>
<tr>
<td>Differential input range</td>
<td>± 80ua</td>
</tr>
<tr>
<td>Differential output @ iout-iout'</td>
<td>±160ua</td>
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<tr>
<td>Linearity error</td>
<td>±0.05ua</td>
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<tr>
<td>Sampling frequency</td>
<td>100MHz</td>
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<tr>
<td>Input frequency linearity error measurement</td>
<td>5MHz</td>
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<tr>
<td>Resolution</td>
<td>12-Bit</td>
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<tr>
<td>Acquisition time</td>
<td>2ns</td>
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<tr>
<td>3dB bandwidth</td>
<td>178MHz</td>
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</table>

VII. CONCLUSION

A high-linearity, low-voltage and high-speed current-mode sample-and-hold circuit has been designed. This circuit design is based on low supply voltage at 1.5V and it utilizes a fully differential circuit. Signal - dependent error is completely eliminated by a new zero voltage switching technique. The circuit has been simulated using a 0.25μm CMOS technology. The circuit has a linearity error equal to ±0.05μa , i.e. 12-bit accuracy with a ±160 μa differential output , input signal frequency of 5MHz , and sampling frequency of 100 MHz. Third harmonic is equal to –78dB. The measured power-dissipation at 1.5V supply-voltage is 2.5mW.

The hold-setting-time and acquisition time are calculated approximately 1.1ns and 2ns.